BST28C64

8K×8bit EEPROM Circuit Product Manual

Table of contents

I. Product Introduction

1.1. Product Overview

The BST28C64 is a 5V powered 8 -bit electrically erasable programmable read-only memory (EEPROM) with a storage capacity of 64Kbit, a read time of less than 200ns, and a CMOS quiescent current of less than 200μA when the device is not selected. It is widely used in system non-volatile data and instruction storage.

BST28C64 bare core adopts imported AT28C64 die.

When programming data using a general-purpose programmer such as Xeltech, ensure that the CATALYST CAT28C64A device is selected in the host computer software; otherwise, programming may fail.

1.2. Features

- Compatible with Xicor's X28C64DBM-20 circuit
- Operating voltage: 5V±0.5V
- Quiescent current: ≤200μA
- Data capacity: 8K×8bit
- Data access time: ≤200ns
- Input and output ports compatible with CMOS and TTL Level
- ESD: ≥500V
- Operating temperature: -55 °C to 125 °C
- Package: CDIP28

1.3. Product use and application range

The chip is suitable for non-volatile data storage and meets the different requirements of military and commercial use.

1.4. Corresponding replacement of foreign products

Benchmarked against Xicor 's X28C64DBM-20 circuit.

II. Product appearance

2.1. Product size

BST28C64 circuit uses a 28-pin ceramic dual-in-line package, and the circuit dimensions are shown in Figure 1.

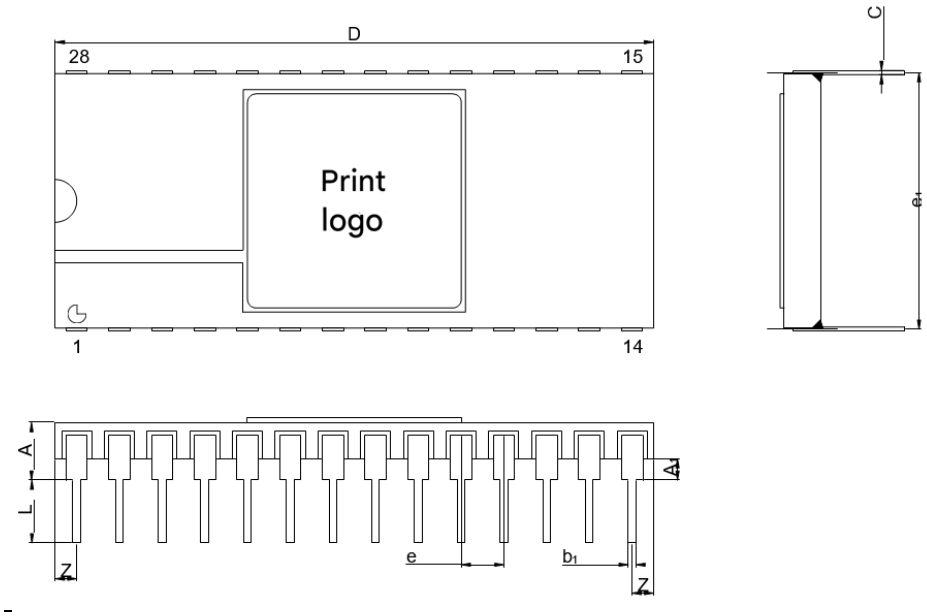

Figure 1. Dimensions

Table 1. Dimensions

DIMENSION SYMBOLS	VALUE MM		
	MINIMUM	NOMINAL	MAXIMUM
A	—	—	5.10
A 1	0.51	—	—
b 1	0.35	—	0.59
c	0.20		0.36
e	—	2.54	—
e 1	—	15.24	—
L	2.54	—	5.00
Z	—	—	2.54
D	—	—	38.10

2.2. Weight

The device weight is 4.8±0.25g.

2.3. Packaging process

The device adopts 0.6μm EEPROM process structure; the capping adopts gold-tin alloy capping process; the marking adopts metal ink pad printing process.

2.4. Product photos and logo descriptions

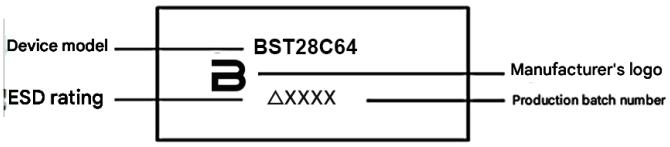

Figure 2. Physical photos and printed logos

Note: The production batch number consists of 4 digits, the first 2 digits represent the year, and the last 2 digits represent the calendar week.

III. Quality assurance level

The product quality grade is implemented according to B1 level specified in GJB 597A-1996, and the assessment standard complies with the requirements of Q/FC 20146-2006 "Detailed Specifications for Semiconductor Integrated Circuit BST28C64 Electrically Erasable Read-Only Memory".

IV. Brief description of basic working principle

4.1. Circuit Function Block Diagram

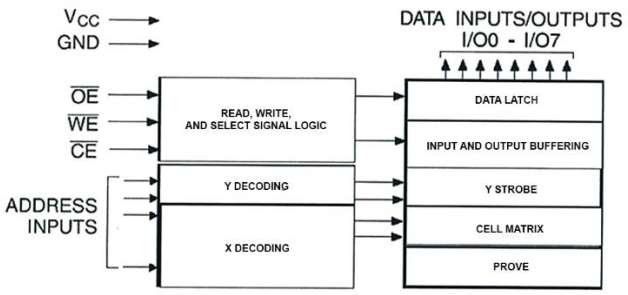

Figure 3. Functional Block Diagram

4.2. Package Pin Description

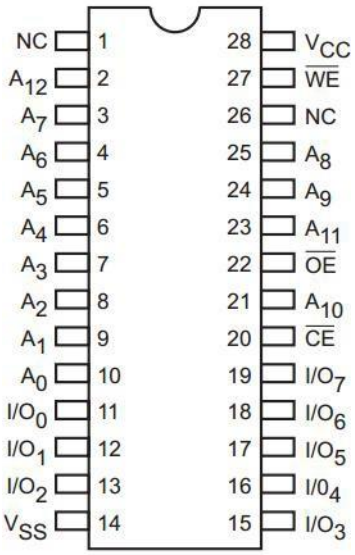

Figure 4 Pin Arrangement

Table 2. Pin Assignment Table

SERIAL NUMBER	SYMBOL	FUNCTION	SERIAL NUMBER	SYMBOL	FUNCTION
1	NC	Empty pin	28	V_{CC}	Power supply
2	A12	Address input	27	$\overline{WE}$	Write enable, low active
3	A7	Address input	26	NC	Empty feet
4	A6	Address input	25	A8	Address input
5	A5	Address input	24	A9	Address input
6	A4	Address input	23	A11	Address input
7	A3	Address input	22	$\overline{OE}$	Output enable, low active
8	A2	Address input	21	A10	Address input
9	A1	Address input	20	$\overline{CE}$	Chip select signal, low effective
10	A0	Address input	19	I/O7	Data Input / Output
11	I/O0	Data Input / Output	18	I/O6	Data Input / Output
12	I/O1	Data Input / Output	17	I/O5	Data Input / Output
13	I/O2	Data Input / Output	16	I/O4	Data Input / Output
14	VSS	GND	15	I/O3	Data Input / Output

V. Extreme working conditions and recommended working conditions

5.1. Extreme working conditions

Table 3. Extreme working conditions

PROJECT	EXTREME WORKING CONDITIONS
Supply voltage (V_{CC})	+7V
DC output current (I_O)	5mA
Temperature range (T_{stg})	-65 ℃～ +150 ℃

5.2. Recommended operating conditions

Table 4. Recommended operating conditions

PROJECT	RECOMMENDED OPERATING CONDITIONS
Supply voltage (V_{CC})	4.5V~5.5V
Operating ambient temperature (T_A)	-55 ℃ ~125 ℃

VI. Main technical parameters

6.1. Electrical characteristics parameters

Table 5. Electrical characteristics parameters

CHARACTERISTIC	SYMBOL	CONDITION UNLESS OTHERWISE SPECIFIED, V_{CC} = 5V -55 ℃ ≤ T A ≤125 ℃	LIMIT VALUE		UNIT
			MINIMUM	MAXIMUM	
Output high level voltage	V_{OH}	I_{OH} = -400μA,	2.4		V
Output low level voltage	V_{OL}	I_{OL} = 2.1mA,		0.4	V
Input high level voltage	V_{IH}		2.0		V
Input low level voltage	V_{IL}			0.8	V
Input high level leakage current	I_{LIH}	V_{IN} = 5.0V	-10	+10	μA
Input low level leakage current	V_{LIL}	V_{IN} = 0.0V	-10	+10	μA
Output high level leakage current	V_{LOH}	V_{OUT} = 5.0 V, $\overline{CE}$ = V_{IH}	-10	+10	μA
Output low level leakage current	V_{LOL}	V $_{OUT}$ = 0 V, $\overline{CE}$ = V_{IH}	-10	+10	μA
Quiescent current 1	I_{SB1}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}, all I/O Ports open, other inputs = V_{IH}		2	mA
Quiescent current 2	I_{SB2}	$\overline{CE}$ = $\overline{WE}$ = V_{DD} - 0.3V, all I/O Ports open, other inputs are arbitrary		200	μA
Dynamic supply current	I_A	$\overline{CE}$= $\overline{OE}$= V_{IL}, $\overline{WE}$ = V_{IH}, all I/O Ports open, address input = 0.4V/2.4V, f=5MHz		60	mA

FUNCTIONAL TIMING					
characteristic	symbol	condition Unless otherwise specified, V_{CC} = 5V -55 ℃ ≤ T A ≤125 ℃	LIMIT VALUE		UNIT
Reading time	R_C	See Figure 5	200		ns
Chip select enable access time	t_{CE}	See Figure 5		200	ns
Address access time	t_{AA}	See Figure 5		200	ns
Output enable access time	t_{OE}	See Figure 5		80	ns
Chip select valid to output valid	t_{LZ}	See Figure 5	0		ns
Read valid to output valid	t_{OLZ}	See Figure 5	0		ns
Chip select invalid to output high impedance	t_{HZ}	See Figure 5		50	ns
Read invalid to output high ancestor	t_{OHZ}	See Figure 5		50	ns
Output remains after address changes	t_{OH}	See Figure 5	0		ns
Write cycle	t_{WC}	See Figures 6, 7, 9, 10		10	ms
Address creation time	t_{AS}	See Figures 6, 7	0		ns
Address hold time	t_H	See Figures 6, 7	100		ns
Write setup time	t_{CS}	See Figures 6, 7	0		ns
Write hold time	t_{CH}	See Figures 6, 7	0		ns
Chip select pulse width	t_{CW}	See Figure 7	100		ns
Read signal high level setup time	t_{OES}	See Figures 6, 7, 9, 10	10		ns
Read signal high level holding time	t_{OEH}	See Figures 6, 7, 9, 10	10		ns
Write signal pulse width	W_P	See Figures 6, 8	100		ns
Write signal high level recovery	t_{WHP}	See Figure 8	200		ns
Data is valid	t_{DV}	See Figures 6 and 7		1	μs
Data creation	t_{DS}	See Figures 6 and 7	50		ns
Data retention	D_H	See Figures 6 and 7	10		ns
Next write cycle delay	t_{DW}	See Figures 9 and 10	10		μs
Byte load cycle	t_{BLC}	See Figure 8	1	100	μs
Note: The voltage is based on GND, and the current flowing into the device terminal is positive.					

7 Application Guide

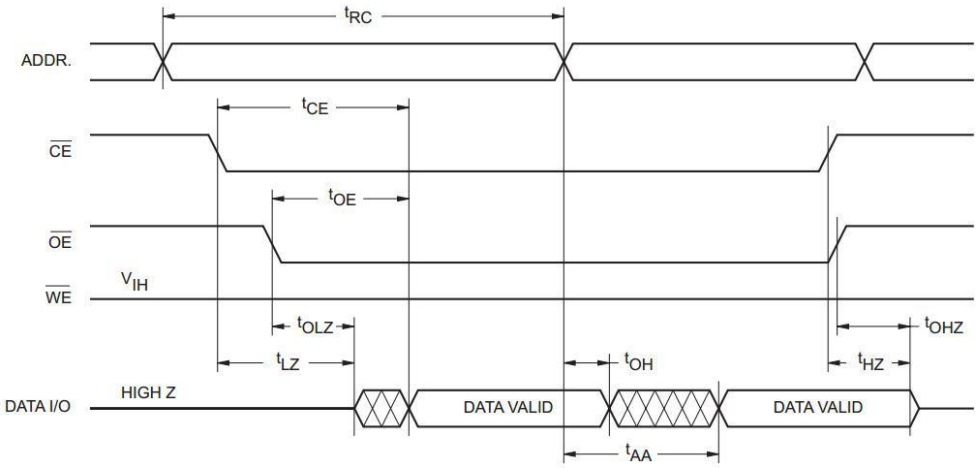

Figure 5. Read cycle

7.1. Key parameter timing diagram / typical application peripherals

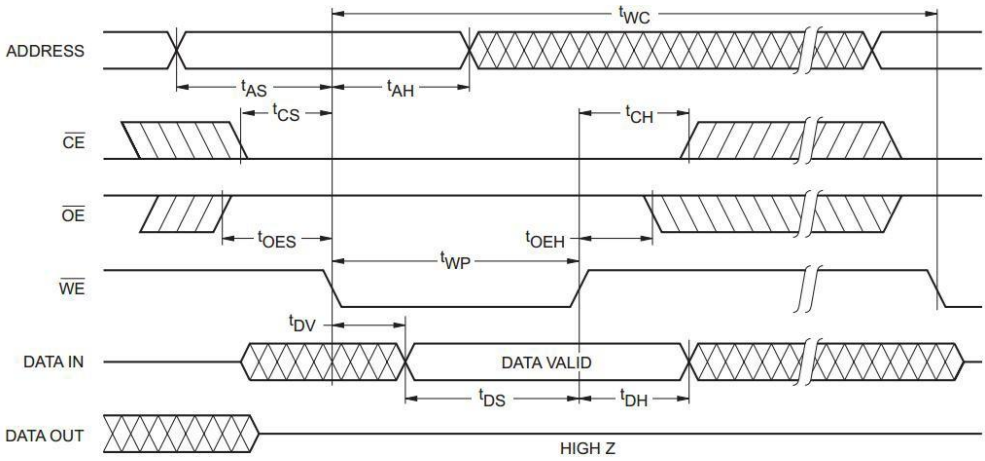

Figure 6. Write cycle controlled by write signal

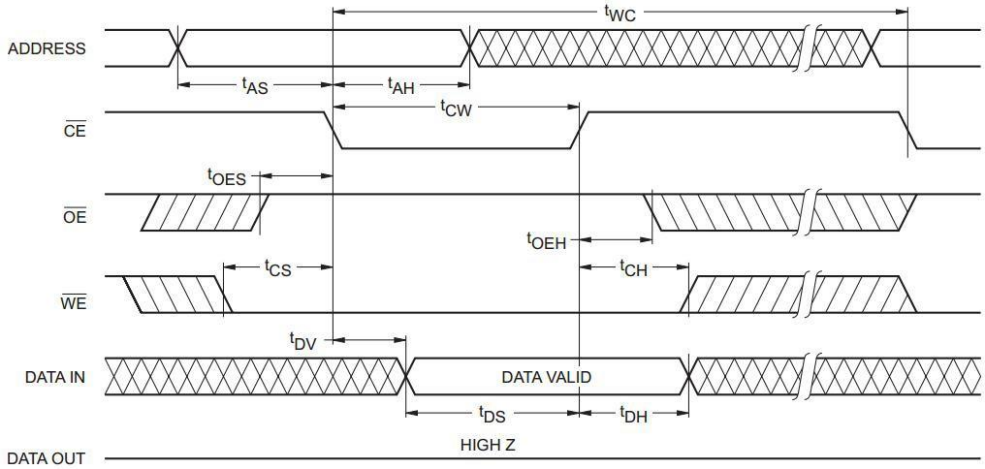

Figure 7. Chip select signal control write cycle

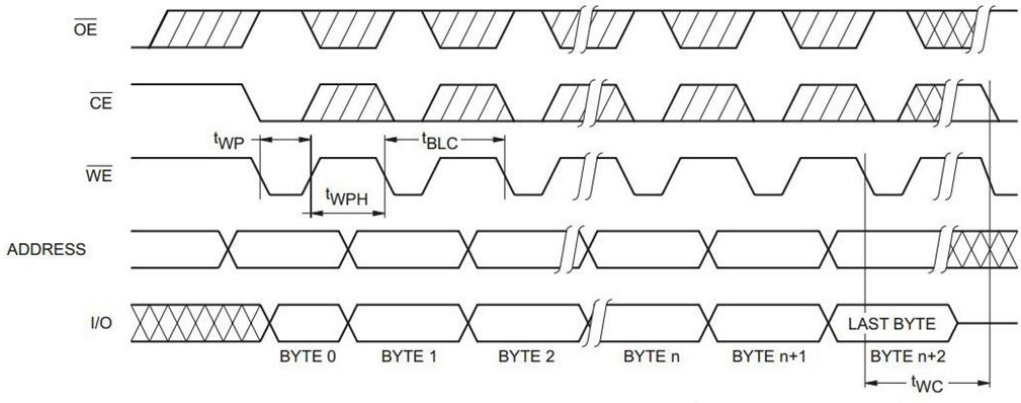

Figure 8 Page Write Cycle

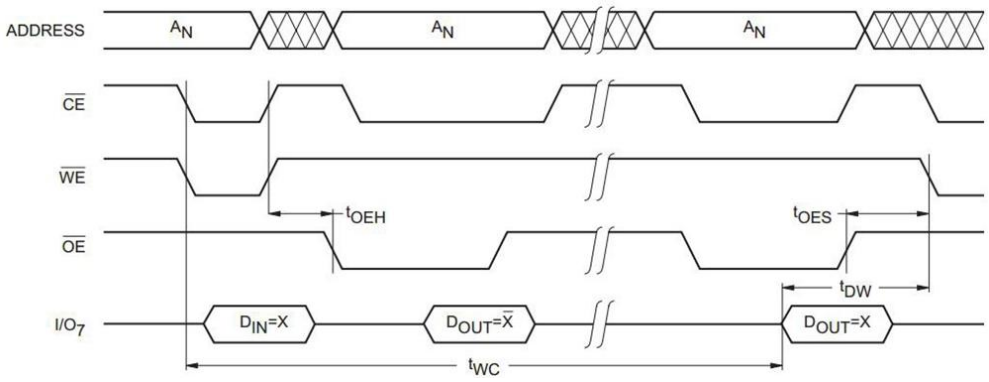

Figure 9. Data polling timing diagram

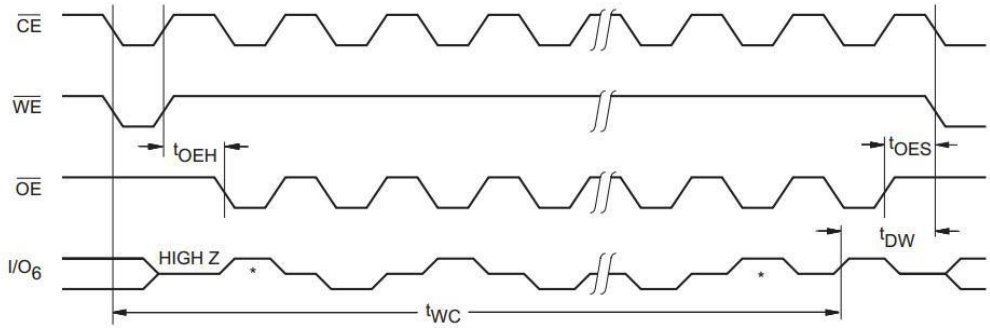

Figure 10. Toggle bit timing diagram

7.2. Circuit Usage Precautions

When this product is used in conjunction with user requirements, if the circuit does not work properly, it is recommended to use the following troubleshooting methods:

- Check whether the power supply voltage supplied to this product on the board meets the requirements;
- Check whether the output level of the output terminal of the interface device on the board meets the input signal level requirements of the product;

- Check whether the input signal in the working mode of this product meets the timing requirements;
- If there is still no correct output signal, please confirm whether the product has been burned out. This product contains ESD, self-protection capability exceeds the Human Body Model (HBM) 500V, but the possibility of damage from electrostatic discharge cannot be ruled out. Both the input and output ports are susceptible to damage by electrostatic discharge.

If the above methods still cannot eliminate the problem, please contact the relevant personnel of the development and production unit immediately.

VII. Precautions

8.1. Product transportation and storage precautions

The product's ambient storage temperature is -65 °C to +150 °C. Use designated anti-static packaging for packaging and transportation. During transportation, ensure the product is protected from collisions with foreign objects. This product should be stored in an air-conditioned environment with controlled temperature and humidity to prevent oxidation of the pins due to prolonged storage, which could affect solderability.

8.2. Product unpacking and inspection

When unpacking the product, please pay attention to the product label on the outer casing. Make sure the product label is clear, without stains or scratches. Also, carefully inspect the outer casing and pins. Make sure the outer casing is not damaged or scratched, and the pins are neatly arranged, not missing, and not deformed.

8.3. Circuit Operation Precautions

This product is an electrostatic sensitive device and should be installed and operated in strict accordance with the operating requirements for electrostatic sensitive devices specified in relevant national standards.

During the installation of this product, it is forbidden to touch or solder this type of product without an anti-static wrist strap or other tools. Do not touch the external leads of the product with your bare hands. Installation and use must be done in an anti-static work area (equipped with an anti-static workbench, tables and chairs, etc.) equipped with an ion blower.

And operate within the effective range of the ion blower.

Operators must undergo anti-static training, wear anti-static work clothes (including anti-static gloves or finger cots, hats, work shoes and anti-static wrist straps), and avoid actions or operations that are likely to generate static electricity.

The anti-static equipment (such as wrist straps and finger cots, etc.) should be tested regularly to ensure that qualified anti-static equipment is used before each use.

Devices should be stored in containers made of static dissipative materials (e.g., special boxes for integrated circuits). Avoid using plastics, rubber, or silk fabrics that may cause static electricity during production, testing, use, and transportation.

Ensure the relative temperature and humidity in the anti-static work area.