BST25QH128 FLASH

Product Brochure

V2.3

Revision History

Serial number	Edition	Change Description	Change order number	Change Person	Change Date	Remark
1	1.0	Initial release	NA	Wang Xin	2018/3/28	
2	2.0	Modify product overview		Yu Gewei	2018/8/3	
3	2.1	Modify the package size		Yu Gewei	2021/4/7	
4	2.2	Modify product model information		Yu Gewei	2021/10/28	
5	2.3	Added instruction tables and equipmentID		Yu Gewei	2022/4/28	

I. Product Overview

BST25QH128 is a 128Mbit serial flash memory with an enhanced write protection mechanism. The device supports a standard serial peripheral interface (SPI), and a high-performance dual/quad output as well as dual/quad I/O using the SPI serial clock, pins: chip select signal, serial DQ0 (DI), DQ1 (DO), DQ2 (WP#) and DQ3 (reset signal). Up to 80MHz SPI clock frequency support allows 160MHz equivalent clock frequency (80MHz×2) dual output and 320MHz (80MHz×4) quad output when using dual/quad I/O fast read instructions.

II. General specification and number

GB/T 7092-1993 Dimensions of semiconductor integrated circuits

GB/T17574-1998 Semiconductor device integrated circuits Part 2: Digital integrated circuits

GJB 548 B-2005 Microelectronic Device Test Methods and Procedures

GJB 7400-2011 General Specification for Semiconductor Integrated Circuits for Qualified Manufacturer Certification

2.1. Detailed specification and confirmation number

Detailed specification number of BST25QH128 model: Q/BST 20385-2018 BST25QH128 model flash memory.

2.2. Testing agency and monitoring test report number

The BST25QH128 testing organization is the Guangzhou Inspection Center for xx electronic components.

2.3. Quality Grade

III. The product quality grade of BST25QH128 is N1.

3.1. Product Basic Information

- Temperature grade requirements
  Working temperature -55℃~125℃, storage temperature -65℃~150℃
- ESD level requirements
  ESD level 2000V
- Power supply working:
  2.7-3.6V
- Serial interface architecture

  SPI compatible: Mode 0 and Mode 3

  - Standard, dual or quad SPI interface
  - Standard SPI: CLK, CS#, DI, DO, WP#, HOLD#
  - Dual SPI: CLK, CS#, DQ 0, DQ 1, WP#, HOLD#
  - Quad SPI: CLK, CS#, DQ 0, DQ1, DQ2, DQ3 Application range:
    - high performance
    - The read operation frequency in standard mode is 83MHz
    - Fast Mode (single data mode rate)
    - Standard SPI: single data bit rate 104MHz clock frequency
    - Dual SPI: Single data bit rate 104MHz clock rate
    - Quad SPI: Three data bit rates 104MHz clock rate

- Low power consumption
  - Typical operating mode power consumption is 5mA
  - Typical power-off power consumption 1uA
- Unified sector architecture
  - -4096 4Kbyte sectors
  - -512 32Kbyte sectors
  - 256 64Kbyte sectors
  - Each sector can be erased individually
  - Write protection function of software and hardware
  - All or part of the data can be write-protected by software
  - Write protection can be enabled/disabled via the WP# pin
  - High-speed programming and erasing
  - The typical programming time for a single page is 0.5ms
  - The typical time for sector erase is 40ms
  - Typical time for half block erase is 200ms
  - The typical time for a block erase is 300ms
  - The typical time for erasing single chip data is 60s
  - Data storage time up to 20 years

IV. Product Pin Information

Pin arrangement diagram:

VDFN8 package

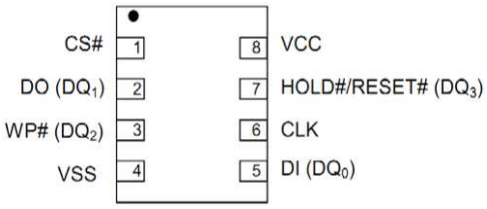

Figure 1. BST25QH128 plastic package VDFN8 pin arrangement

Pin definition:

The following is the description of the functions of each pin of BST25QH128:

Logo	Definition
CLK	Serial clock input
DI	Serial data inputD1
DO	Serial data inputD0
CS#	Chip select enable
WP#	Write protection
HOLD#/RESET#	Reset or hold signal
Vcc	power supply
Vss	land

Note:

- DQ0 and DQ1 are used in dual and quad modes.
- DQ0~DQ3 are only used in quad mode, WP# & HOLD# (or RESET#) are only used in standard or dual mode.

Pin Function Description

- Serial data input and output (DI, DO and DQ0, DQ1, DQ2, DQ3)
  BST25QH128 supports standard SPI interface, dual SPI and quad SPI operation. Standard SPI instructions use the unidirectional D0 (input) pin to serially write instructions unidirectional address or data on the rising edge of the serial clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status on the falling edge CLK.
  Dual and Quad SPI instructions use bidirectional IO pins to serially write instructions, addresses, or data into the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.
- Serial clock (CLK)
  The SPI serial clock input (CLK) pin provides serial input and output operation.
  Chip Select (CS#)
  The SPI Chip Select (CS#) pin enables and disables operation. When CS# is high, the device is disabled and the serial data output (D0 or DQ 0, DQ 1, DQ 2

and DQ 3) pins are high impedance. When the device is disabled, the device power consumption is at the standby level unless an erase, program and status register cycle is in progress. When CS# is pulled low, the device is selected, the power consumption increases to the normal working state and data can be written and read normally. After power-on, the CS# signal must change from high to low before a new instruction is input.

- Hold (HOLD#)
  The HOLD# pin allows the device to be suspended while in operation. HOLD# is enabled when WXDIS and HRSW are low. When HOLD# and CS# are low, the DO pin is in high impedance state, and the D1 and CLK signals are ignored. When in Quad SPI, this pin is used for the serial data IO (DQ 3) for quad I/O operation.
- Write Protect (WP#)
  The Write Protect (WP#) pin can be used to prevent the status register from being written. Used with the Status Register Protection Block (BP0, BP1, BP2, and BP3) bits and the Status Register Protect (SRP) bit, part or the entire memory array can be hardware protected. This WP# function is only available for standard SPI and dual SPI operations. When in quad SPI, this pin is used for serial data IO (DQ 2) as quad I/O operation.

V. Memory Function Description

BST25QH128 storage module

- 16777216 Byte
- Storage module architecture can be divided into the following types
  - 256 64 Kbyte modules
  - 512 32 Kbyte modules
  - 4096 4 Kbyte sectors
  - 65536 pages (256 bytes per page)

Each page of this memory can be programmed with either 0 or 1.

Schematic diagram:

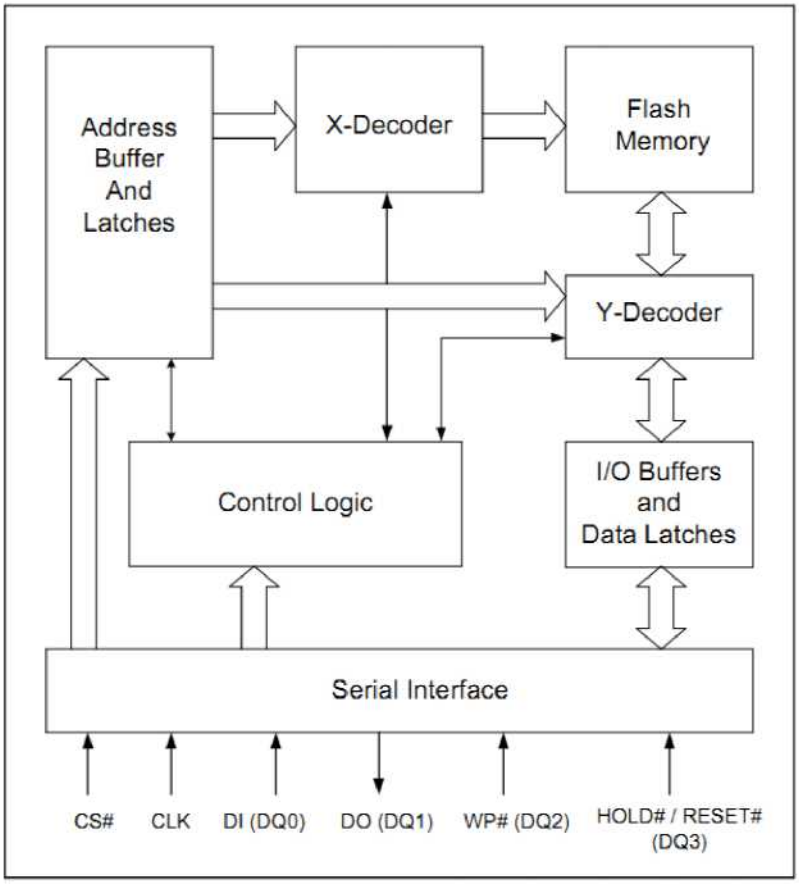

Figure 5. BST25QH128 block diagram

The block or sector storage structure of the device:

64K Block	32K Block	Sector	Address range	
255	511	4095	FFFOOOh	FFFFFFh
	510	4080	FFOOOOh	FFOFFFh
254	509	4079	FEFOOOh	FEFFFFFh
	508	4064	FEOOOOh	FEF
253	507	4063	FDFOOOh	FDFFFFh
	506	4048	FDOOOOh	FDOFFF
242	485	3887	F2F000h	F2FF

	484	3872	F20000h	F20FFF
241	483	3871	FIFOOOh	FIFFFFh
	482			
		3856	FlOOOO	FWf
240	481	3855	FOFOOOh	FFF
	480			
		3840	FOOOOOh	FOOFFFh
64K Block	32K Block	Sector	Address range	
239	479	3839	EFFOOOh	EFFFFFh
	478			
		3824	EFOOOOh	EFOFFF
238	477	3823	EEFOOOh	EEFFF
	476			
		3808	EEOOOOh	EEEOFFF
237	475	3807	EDFOOOh	EDFFFh
	474			
		3792	EDOOOOh	EDFH
226	453	3631	E2F000h	E2FFFF
	452			
		3616	E20000h	E20FFF
225	451	3615	EIFOOOh	E
	450			
		3600	EWO	EW
224	449	3599	EOFOOOh	EOFFFF
	448			
		3584	EOOOOOh	EOOFFF

64K Block	32K Block	Sector	Address range	
223	447	3583	DFFOOOh	DFFFFFh
	446			
		3568	DFOOOOh	DFOFF
222	445	3567	DEFOOOh	DEFFFF
	444			
		3552	DEOOOOh	DEOFFF
221	443	3551	DDFOOOh	DDFFFFh
	442			
		3536	DDOOOOh	DDOFFF
210	421	3375	D2F000h	D2F
	420			
		3360	D20000h	D20FFF
209	419	3359	DIFOOOh	DIFFFFh
	418			
		3344	DIOOOOh	WIFF
208	417	3343	DOFOOOh	DOFFFF

	416			
		3328	DOOOOOh	DOOFFFh
64K Block	32K Block	Sector	Address range	
207	415	3327	CFFOOOh	CFFFFFh
	414			
		3312	CFOOOOh	CFOFFF
206	413	3311	CEFOOOh	CEFFFFh
	412			
		3296	CEOOOOh	CEOFFF
205	411	3295	CDFOOOh	CDFFFF
	410			
		3280	CDOOOOh	CDOFF
194	389	3119	C2F000h	C2F
	388			
		3014	C20000h	C20FFF
193	387	3103	CIFOOOh	CIFFF
	386			
		3088	CWOOO	FWf
192	385	3087	COFOOOh	COFFFF
	384			
		3072	COOOOOh	COF
64K Block	32K Block	Sector	Address range	
191	383	3071	BFFOOOh	BFFFFF
	382			
		3056	BFOOOOh	Ff
190	382	3055	BEFOOOh	BEFFFFh
	380			
		3040	BEOOOOh	BEOFFF
189	379	3039	BDFOOOh	BDFFFF
	378			
		3024	BDOOOOh	BDFF
178	357	2863	B2F000h	BfFF
	356			
		2848	B20000h	B20FFF
177	355	2847	BIFOOOh	BIFFFFh
	354			
		2832	BWOOO	BIOFF
176	353	2831	BOFOOOh	BOFFFF
	352			
		2816	BOOOOOh	BOOFFF
64K Block	32K Block	Sector	Address range	
175	351	2815	AFFOOOh	AFFFFFh
	350			
		2800	AFOOOOh	AFOFFF

174	349	2799	AEFOOOh	AEFFFF
	348	2784	AEOOOOh	FWf
173	347	2783	ADFOOOh	ADFFFF
	346	2768	ADOOOOh	ADOFF
162	325	2607	A2F000h	AHr
	324	2592	A20000h	A20FFF
161	323	2591	AIFOOOh	AIFFFF
	322	2576	AWOOOh	WFFF
160	321	2575	AOFOOOh	AOFFFF
	320	2560	AOOOOOh	AOOFFF

64K Block	32K Block	Sector	Address range	
159	319	2559	9FF000h	QFFFF
	318	2544	QFOOOOh	9F0FFFh
158	317	2543	9EF000h	QEFFFF
	316	2528	9E0000h	QUR
157	315	2527	9DF000h	SDFFFFh
	314	2512	9D0000h	9D0FFF
146	293	2351	92F000h	92FFFFh
	292	2336	920000h	920FFFh
145	291	2335	SIFOOOh	91FFFFh
	290	2320	910000h	910FFFh
144	289	2319	SOFOOOh	90FFFFh
	288	2304	900000h	900FFFh
64K Block	32K Block	Sector	Address range	
143	287	2303	8FF000h	8FFFFFFh
	286	2288	8F0000h	8F0FFFh
142	285	2287	8EF000h	8EFFFFh

	284	2272	8E0000h	8E0FFFh
141	283	2271	8DF000h	SDFFFFh
	282	2256	8D0000h	8D0FFFh
130	261	2095	82F000h	82FFFFh
	260	2080	820000h	820FFFh
129	259	2079	81F000h	81FFFFh
	258	2064	810000h	810FFFh
128	257	2063	80F000h	80FFFFh
	256	2048	800000h	800FFFh

64K Block	32K Block	Sector	Address range	
127	255	2047	7FF000h	7FFFFF
	254			
		2032	7F0000h	7F0FFF
126	253	2031	7EF000h	7EFFFFh
	252			
		2016	7E0000h	7E0FFFh
125	251	2015	7DF000h	7DFFFF
	250			
		2000	7D0000h	7D0FFF
114	229	1839	72F000h	72FFFFh
	228			
		1824	720000h	720FFFh
113	227	1823	71F000h	71FFFFh
	226			
		1808	710000h	710FFFh
112	225	1807	70F000h	70FFFFh
	224			
		1792	700000h	700FFFh
64K Block	32K Block	Sector	Address range	
111	223	1791	6FF000h	6FFFFFh
	222			
		1776	6F0000h	6F0FFFh
110	221	1775	6EF000h	6EFFFFh
	220			
		1760	6E0000h	6E0FFFh
109	219	1759	6DF000h	6DFFFF

	218	1744	6D0000h	6D0FFF
98	197	1583	62F000h	62FFFFh
	196			
		1568	620000h	620FFFh
97	195	1567	61F000h	61FFFFh
	194			
		1552	610000h	610FFFh
96	193	1551	60F000h	60FFFFh
	192			
		1536	600000h	600FFFh

64K Block	32K Block	Sector	Address range	
95	191	1535	5FF000h	5FFFFFFh
	190			
		1520	5F0000h	5F0FFFh
94	189	1519	5EF000h	5EFFFFh
	188			
		1504	5E0000h	5E0FFFh
93	187	1503	5DF000h	5DFFFFh
	186			
		1488	5D0000h	5D0FFF
82	165	1327	52F000h	52FFFFh
	164			
		1312	520000h	520FFFh
81	163	1311	51F000h	51FFFFh
	162			

		1296	510000h	510FFFh
80	161	1295	50F000h	50FFFFh
	160			
		1280	500000h	500FFFh
64K Block	32K Block	Sector	Address range	
79	159	1279	4FF000h	4FFFFFFh
	158			
		1264	4F0000h	4F0FFFh
78	157	1263	4EF000h	4EFFFFh
	156			
		1248	4E0000h	4E0FFFh
77	155	1247	4DF000h	4DFFFF
	154			
		1232	4D0000h	4D0FFF
66	133	1071	42F000h	42FFFFh
	132			
		1056	420000h	420FFFh
65	131	1055	41F000h	41FFFFh
	130			
		1040	410000h	410FFFh
64	12S	1039	40F000h	40FFFFh
	128			
		1024	400000h	400FFFh
64K Block	32K Block	Sector	Address range	
63	127	4095	3FF000h	3FFFFFh

	126			
		4080	3F0000h	3F0FFFh
62	125	4079	3EF000h	3EFFFFh
	124			
		4064	3E0000h	3E0FFFh
61	123	4063	3DF000h	3DFFFF
	122			
		4048	3D0000h	3D0FFFh
50	101	815	32F000h	32FFFFh
	100			
		800	320000h	320FFFh
49	99	799	31F000h	31FFFFh
	98			
		784	310000h	310FFFh
48	97	783	30F000h	30FFFFh
	96			
		768	300000h	300FFFh
64K Block	32K Block	Sector	Address range	
47	95	767	2FF000h	2FFFFFh
	94			
		752	2F0000h	2F0FFFh
46	93	751	2EF000h	2EFFFFh
	92			
		736	2E0000h	2E0FFFh
45	91	735	2DF000h	2DFFFFh

	90			
		720	2D0000h	2D0FFFh
34	69	559	22F000h	22FFFFh
	68			
		544	220000h	220FFFh
33	67	543	21F000h	21FFFFh
	66			
		528	210000h	210FFFh
32	65	527	20F000h	20FFFFh
	64			
		512	200000h	200FFFh

64K Block	32K Block	Sector	Address range	
31	63	511	IFFOOOh	IFFFFFh
	62			
		496	IFOOOOh	IFOFFF
30	61	495	1EF000h	EFFFF
	60			
		480	1E0000h	f
29	59	479	IDFOOOh	IDFFFF
	58			
		464	IDOOOOh	WFh
18	37	303	12F000h	12FFFFh
	36			
		288	120000h	120FFFh

17	35	287	11F000h	11FFFFh
	34			
		272	110000h	110FFFh
16	33	271	WFOO	WFFF
	32			
		256	100000h	f
64K Block	32K Block	Sector	Address range	
15	31	255	OFFOOOh	OFFFFF
	30			
		240	OFOOOOh	OFOFFF
14	29	239	OEFOOOh	OEFFFF
	28			
		224	OEOOOOh	OEOFF
13	27	223	ODFOOOh	ODFFFFh
	26			
		208	ODOOOOh	ODOFFF
2	5	47	02F000h	02FFFFh
	4			
		32	020000h	020FFFh
1	3	31	OlFOOOh	Ol
	2			
		16	OlOOOOh	DIOFFF
0	1	15	OOFOOOh	OOFFFF
	0			
		0	OOOOOOh	ODOFFF

Command and device ID:

Instruction Name	Bytel Code	Byte 2	Byte3	Byte4	Byte 5	Byte 6	n-Bytes
RSTEN	66h						
RST（1）	99h						
EQPI	38h						
rstqpM)	FWf						
Write Enable (WERN)	06h						
Volatile Status Register Write Enable (3)	50h						
Write Disable (WRDI)/ Exit OTP mode	04h						
Read Status Register (RDSR)	05h	(S7-S0)(4)					continuous^)
Write Status Register (WRSR)	01h	S7-S0					
Read Status Register 3 (RDSR3)	95h	(S7-S0)(4)					
Write Status Register 3 (WRSR3)	COh	S7-S0					
Deep Power-down	B9h						
Release from Deep Power-down, and read Device ID (RES)	ABh	dummy	dummy	dummy	(ID7-ID0)		(6)
Release from Deep Power-down (RDP)							
Manufacturer/ Device ID	90h	dummy	dummy	Oh	(M7-M0)	(ID7-ID0)	(7)
				oeLh	(ID7-ID0)	(M7-M0)	
Read Identification (RDID)	9F	(M7-M0)	(ID15 - ID8)	(ID7-ID0)	(8)		
Enter OTP mode	3Ah						
Read SFDPmodeand Unique ID Number	5Ah	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(Next Byte) continuous

VI. Electrical characteristics

DC parameters:

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Li	Input Leakage Current			1	±2	pA
Lo	Output Leakage Current			1	±2	pA
'cci	Standby Current	CS#=VCCV|N=Vss orvcc			20	pA
6c2	DeepPower-down Current	CS# 2Vcc, V|NtwoVss°vcc			20	M
ba	Operating Current (READ)	CLK=0.1 Vcc/0.9 Vcc al 104MHz, DQ=open		10	25	mA
		CLK=0.1 Vcc/0.9 Vcc at 33MHz, DQ=open		5	12	mA
		CLK=0.1Vcc/0.9Vcc104MHz, Quad Output Read, DQ=open		14	35	mA
		CLK=0.1 Vcc/0.9 Vcc at33MHz,Quad Output Read, DQ=open		7	17	mA
Icc4	Operating Current (PP)	CS# = VCC		9	30	mA
'CC5	Operating Current (WRSR)	CS# =vcc			25	mA
Ьсб	Operating Current (SE)	CS#=vcc		13	25	mA
■CC7	Operating Current (BE)	CS#=vcc		15	25	mA
V|L	InputLowVoltage		-0.5		0.2 VCC	V
VIH	Input High Voltage		Q・7Vcc		Vcc+0・4	V
v0L	OutputLowVoltage	l°L=100 pA, Vcc=VccMin.			0.3	V
v0H	Output High Voltage	IOH=-100 pA,Vcc=VccMin.	Vcc-0.2			V

Note:

The above parameters are tested under -55C°0T$125°C, VCC = 2.7~3.6V conditions.AC parameters:

Symbol	Alt	Parameter	Min	Type	Max	Unit
		Serial SPI Clock Frequency for: PP, QPP, SE, HBE, BE, CE, DP, RES, RDP, WREN, WRDI, WRSR, WRSR3, Fast Read	DC.		104	MHz
F		Serial SPI Clock Frequency for: RDSR, RDSR3, RDID,	DC		104	MHz
rR	%	Serial Dual/Quad Clock Frequency for: PP, QPP, SE, HBE, BE, CE, DP, RES, RDP, WREN, WRDI, WRSR, WRSR3, RDSR, RDSR3, RDID, Fast Read. Dual Output Fast Read, Dual I/O	DC		104	MHz

		Fast Read. Quad I/O Fast Read				
^R		Serial Clock Frequency for READ	DC		83	MHz
^н 1		Serial Clock High Time	3.5			ns
GJ		Serial Clock Low Time	3.5			ns
QUR		Serial Clock Rise Time (Slew Rate)	0.1			V/ns
^CHCL2		Serial Clock Fall Time (Slew Rate)	0.1			V/ns
4lch	kss	CS# Active Setup Time	5			ns
&SH		CS# Active Hold Time	5			ns
Цнсн		CS# Not Active Setup Time	5			ns
&SL		CS# Not Active Hold Time	5			ns
bNb	&H	CS# High Time for read CS# High Time for program/erase	30 30			ns
^SHSL2	&H	Volatile Register Write Time	50			ns
tqZ	'DIS	Output Disable Time			6	ns
QUR	Go	Output Hold Time	0			ns
bv	%su	Data In Setup Time	2			ns
ikB	,DH	Data In Hold Time	3			ns
44LCH		HOLD#LowSetup Time(relative to CLK)	5			ns
^HHCH		HOLD# High Setup Time (relative to CLK)	5			ns
&HH		HOLD# Low Hold Time(relative to CLK)	5			ns
X:HHL		HOLD# High Hold Time (relative to CLK)	5			ns
LqCy	q	Output Valid from CLK			7	ns
^VHSL		Write Protect Setup Time before CS# Low	20			ns
oeLh		Write Protect Hold Time after CS# High	100			ns
%p2		CS# High to Deep Power-down Mode			3	PS
^RES1		CS# High to Standby Mode without Electronic Signature read			:	№
'RE$2 5		CS# High to Standby Mode with Electronic Signature read		10	50	MS ms
		Write Status Register Cycle Time				
tpp		Page Programming Time		0.5	3	ms
Це		Sector Erase Time		0.04	0.3	s
^HBE		Half Block Erase Time		0.2	1	s
'BE		Block Erase Time		0.3	2	s
,CE		Chip Erase Time		60	200	s
^HRST		RESET# low period to reset the device	1			Ms
^HRSL		RESET# high to next instruction	28			us
^SHRV		Deselect to RESET# valid in quad mode	8			ns
		Software Reset	WIP=write operation			28	us

	Ar	Latency	WIP=not in write operation			0	5

Note:

The above parameters are tested under -55C°0T$125°C, VCC = 2.7~3.6V conditions.

VII. Package size

VDFN8(6*8mm):

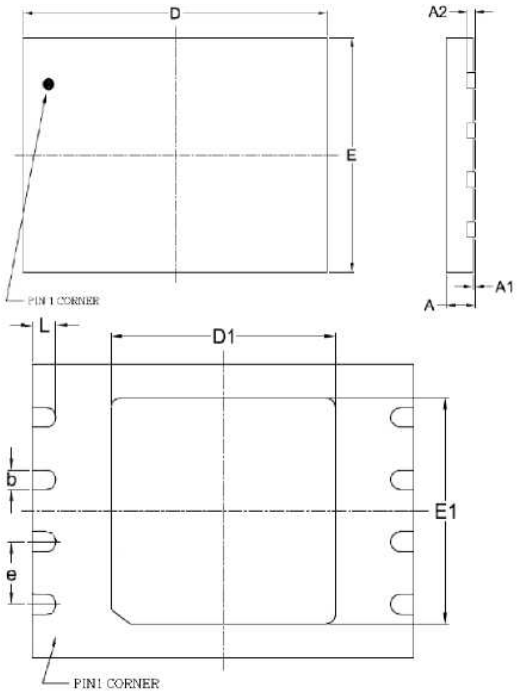

Figure 7-1. VDFN8 (6*8mm) dimensions

Dimension symbols	Value (in millimeters)		
	Minimum	Nominal	maximum
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	-	0.20	-
D	7.90	8.00	8.10
E	5.90	6.00	6.10
D1	3.35	3.40	3.45
E1	4.25	4.30	4.35
e	-	1.27	-
b	0.35	0.40	0.48

L	0.4	0.50	0.60

VIII. Product Information

BST 25QH128

- 25QH128 represents the product model

Product Ordering Information

Product Model	Package	Packaging materials	Quality Grade	Detailed specifications	Product Status
BST25QH128	VDFN8	plastic	N1class	Q/BST 20412-2018	Mass production