# BST24C512

# 2- wire serial EEPROM

# Product Manual

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## I. Overview

The BST24C512 is a 512K-bit serial electrically erasable programmable read-only memory (EEPROM). The memory is organized as 65536 x 8 bits, divided into 512 pages of 128 bytes each. It features an I2C interface and is suitable for low-power, low-voltage systems.

Its main features are as follows:

- Write protect pin provides hardware data protection
- Wide operating voltage range: 1.8V ~ 5.5V
- The internal structure of the memory is: 65536×8 (512K)
- Two-wire serial interface
- Schmitt trigger to suppress input noise

- Bidirectional data transmission protocol
- 400 kHz (1.8V ~ 2.5V) and 1MHz (2.5V ~ 5.5V) clock range
- 128-byte Page Write
- Allow partial page write operations
- Additional write-locked pages
- Self-timed write cycle (5ms max)
- High reliability:
  - Erase and write times: 1 million times;
  - Data retention: 100 years
- Package: DIP8 \SOP8 \TSSOP8

**Ordering Information:**

**Tube:**

Table 1

| PRODUCT NUMBER | PACKAGE | PRINT LOGO | PCS PER TUBE | TUBES PER BOX | PCS PER BOX | NOTES |
|---|---|---|---|---|---|---|
| BST24C512DA8.TB | DIP8 | 24C512 | 50 | 40 | 2 000 | Plastic package size: 9.2mm×6.4mm Pin spacing: 2.54mm |
| BST24C512SA8.TB | SOP8 | 24C512 | 100 | 100 | 10 000 | Plastic package size: 4.9mm×3.9mm Pin spacing: 1.27mm |
| BST24C512TB8.TB | TSSOP8 | 24C512 | 100 | 200 | 20 000 | Plastic package size: 3.0mm×4.4mm Pin spacing: 0.65mm |

**Taping:**

Table 2

| PRODUCT NUMBER | PACKAGE | PRINT LOGO | PCS per REEL | PCS per BOX | NOTES |
|---|---|---|---|---|---|
| BST24C512SA8.TR | SOP8 | 24C512 | 4 000 | 8 000 | Plastic package size: 4.9mm×3.9mm Pin spacing: 1.27mm |
| BST24C512TB8.TR | TSSOP8 | 24C512 | 5 000 | 10 000 | Plastic package size: 3.0mm×4.4mm Pin spacing: 0.65mm |

Note: If the actual product is inconsistent with the order information, please refer to the actual product.

# II. Functional block diagram and pin description

## 2.1. Functional Block Diagram

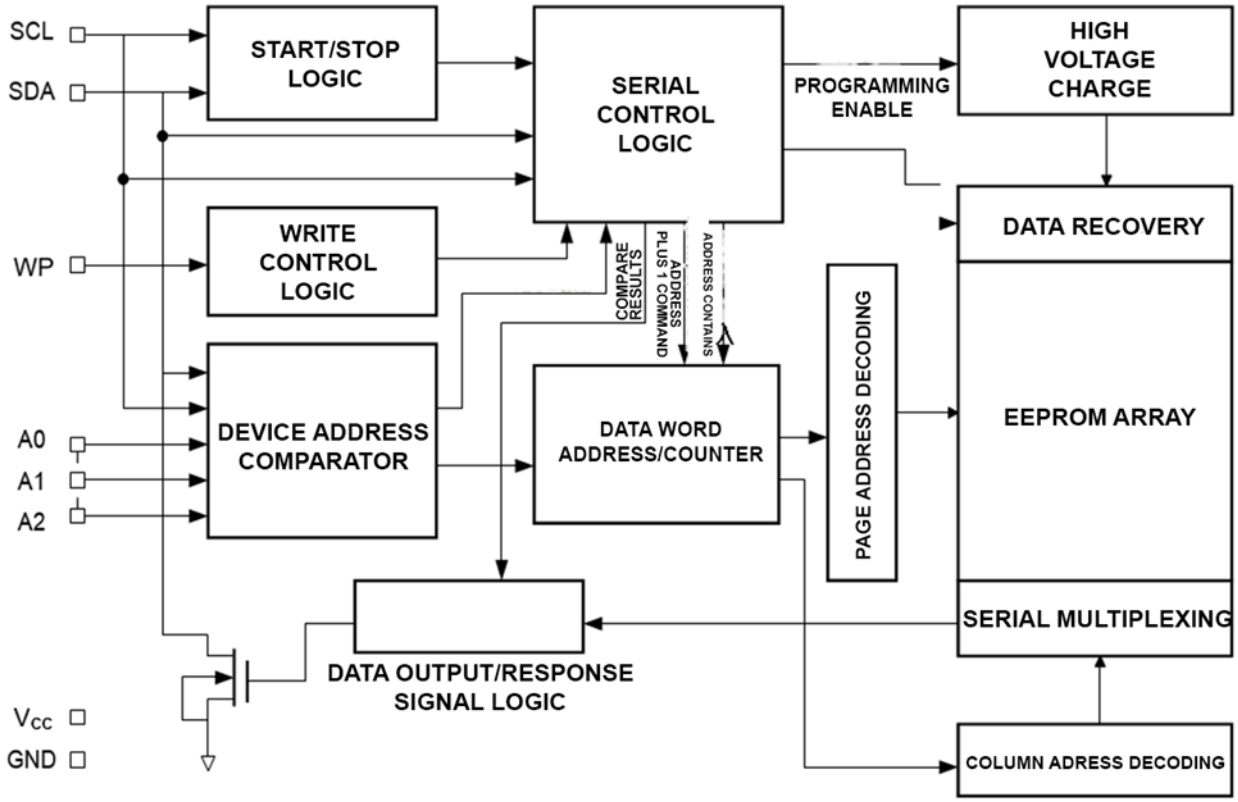


Figure 1. Functional block diagram

## 2.2. Pin arrangement diagram

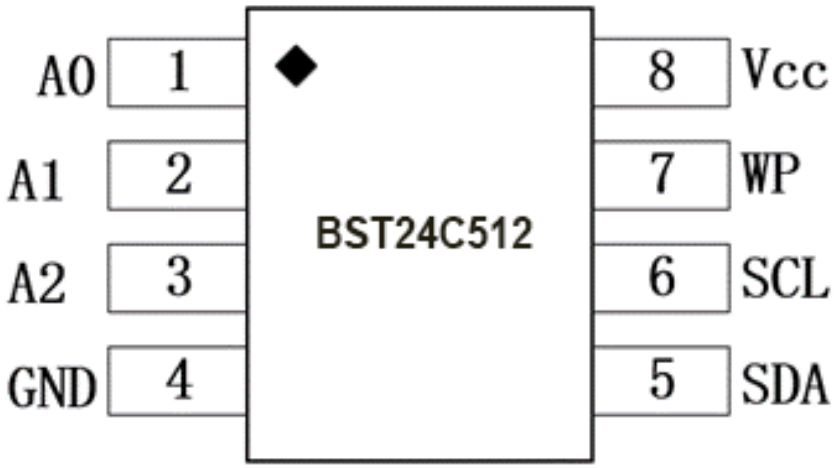


Figure 2. Pinout

### 2.3. Pin Description

Table 3.

| PINOUT | SYMBOL | FUNCTION |
|---|---|---|
| 1 | A0 | Device address input:<br>A2, A1 and A0 Pins are device address inputs. Typically, A2, A1 and A0 pins are used for hardware addressing, and a total of 8 can be connected on a single bus system If these pins are left floating, A2, A1 and the A0 pin will be pulled down to GND internally. |
| 2 | A1 | |
| 3 | A2 | |
| 4 | GND | Grounding |
| 5 | SDA | Serial Data:<br>SDA pin is a bidirectional port for data transmission. This pin is open-drain driven and can be wired-ORed with any number of other open-drain or open-collector devices. |
| 6 | SCL | Serial Clock:<br>On the rising edge of the SCL clock, data is sent to the EEPROM ; on the falling edge of the SCL clock, data is sent from the EEPROM.<br>EEPROM sent out. |
| 7 | WP | Write protection:<br>The WP pin can provide hardware data protection. When the WP pin is grounded, normal read / write operations are allowed.<br>WP to $V_{CC}$, write protection is performed. |
| 8 | $V_{CC}$ | Power supply |

Table 4.

| WRITE PROTECTION STATUS | WRITE-PROTECTED PART |
|---|---|
| Connect to $V_{CC}$ | All (128K) |
| Connect to GND | Normal read / write operations |

## III. Electrical characteristics

### 3.1. limit parameters

(Unless otherwise specified, $T_{amb}$ = 25 °C)

Table 5.

| PARAMETER NAME | SYMBOL | CONDITION | RATING | UNIT |
|---|---|---|---|---|
| Power supply voltage | $V_{CC}$ | — | 6.25 (max.) | V |
| DC output current | I | — | 5.0 | mA |
| Voltage on any pin relative to ground | V | — | -1.0 ～ +7.0 | V |
| Input / output capacitance (SDA) | $C_{I/O}$ | $T_{amb}$ =25 ℃, f=1.0MHz,<br>$V_{CC}$ =5V, $V_{I/O}$ =GND, Note 1 | 8 (max.) | pF |
| Input capacitance (A0, A1, A2, SCL) | $C_{IN}$ | $T_{amb}$ =25 ℃, f=1.0MHz,<br>$V_{CC}$ =5V, $V_{I/O}$ =GND, Note 1 | 6 (max.) | pF |

| PARAMETER NAME | SYMBOL | CONDITION | | RATING | UNIT |
|---|---|---|---|---|---|
| Working temperature | $T_{amb}$ | — | | -40 to +85 | ℃ |
| Storage temperature | $T_{STG}$ | — | | -65 to +150 | ℃ |
| Soldering temperature | $T_L$ | 10 seconds | DIP | 250 | ℃ |
| | | | SOP/TSSOP | 260 | |

Note:

- These parameters are characteristic values, not 100% measured values.
- Using the device beyond its operating limits may cause permanent damage. The above ranges are only the main ranges and do not include other unmentioned situations. Extended use at extreme values may affect device reliability.

## 3.2. Electrical characteristics

### 3.2.1. DC parameters

(Unless otherwise specified, $T_{amb}$ = -40 °C to +85 °C $V_{CC}$ = +1.8V $_{to}$ + 5.5V)

Table 6.

| PARAMETER NAME | SYMBOL | TEST CONDITIONS | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| Operating voltage | $V_{CC}$ | — | 1.8 | — | 5.5 | V |
| Working current | $I_{CCR}$ | $V_{CC}$ = 5.5V, 400kHz read operation | — | 0.2 | 0.4 | mA |
| Working current | $I_{CCW}$ | $V_{CC}$ = 5.5V, 400kHz write operation | — | 0.8 | 1.6 | mA |
| Standby current | $I_{SB1}$ | $V_{CC}$ = 3.3V, VIN = $V_{CC}$ or $V_{SS}$, $T_{amb}$ = 85 ℃ | — | — | 1.0 | μA |
| Standby current | $I_{SB2}$ | $V_{CC}$ = 3.3V, VIN = $V_{CC}$ or $V_{SS}$, $T_{amb}$ = 85 ℃ | — | — | 2.0 | μA |
| Input leakage current | $I_{LI}$ | $V_{IN}$ =$V_{CC}$ or GND | — | 0.10 | 1.0 | μA |
| Output leakage current | $I_{LO}$ | $V_{OUT}$ = $V_{CC}$ or GND | — | 0.05 | 1.0 | μA |
| Input low level(1) | $V_{IL}$ | — | -0.6 | — | 0.3$V_{CC}$ | V |
| Input high level(1) | $V_{IH}$ | — | 0.7V $_{CC}$ | — | $V_{CC}$ +0.5 | V |
| Output low level | $V_{OL2}$ | $I_{OL}$ =2.1mA, $V_{CC}$ =3.0V | — | — | 0.4 | V |
| Output low level | $V_{OL1}$ | $I_{OL}$ = 1.5mA, $V_{CC}$ = 1.8V | — | — | 0.2 | V |

Note: $V_{IL}$ Minimum value and $V_{IH}$ The maximum value is a reference value, not a test value.

### 3.2.2. AC parameters

Unless otherwise specified, $T_{amb}$ = -40 ℃ ～ +85 ℃ $V_{CC}$ = +1.8V ～ +5.5V $C_L$ = 100pF)

Table 7.

| PARAMETER NAME | SYMBOL | TEST CONDITIONS | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| Clock frequency, SCL | $f_{SCL}$ | $V_{CC}$=1.8V | — | — | 400 | kHz |
| | | $V_{CC}$=2.7V | — | — | 1000 | |
| | | $V_{CC}$=5V | — | — | 1000 | |
| Clock Pulse Width Low | $t_{LOW}$ | $V_{CC}$=1.8V | 1.3 | — | — | μs |
| | | $V_{CC}$=2.7V | 0.4 | — | — | |
| | | $V_{CC}$=5V | 0.4 | — | — | |
| Clock Pulse Width High | $t_{HIGH}$ | $V_{CC}$=1.8V | 0.6 | — | — | μs |
| | | $V_{CC}$=2.7V | 0.4 | — | — | |
| | | $V_{CC}$=5V | 0.4 | — | — | |
| Noise suppression time (1) | $t_I$ | $V_{CC}$=1.8V | — | — | 100 | ns |
| | | $V_{CC}$=2.7V | — | — | 50 | |
| | | $V_{CC}$=5V | — | — | 50 | |
| Clock low to data output valid | $t_{AA}$ | $V_{CC}$=1.8V | 0.05 | — | 0.9 | μs |
| | | $V_{CC}$=2.7V | 0.05 | — | 0.55 | |
| | | $V_{CC}$=5V | 0.05 | — | 0.55 | |
| the bus must be released before the next value can be transmitted (2) | $t_{BUF}$ | $V_{CC}$=1.8V | 1.3 | — | — | μs |
| | | $V_{CC}$=2.7V | 0.5 | — | — | |
| | | $V_{CC}$=5V | 0.5 | — | — | |
| Start condition hold time | $t_{HD.STA}$ | $V_{CC}$=1.8V | 0.6 | — | — | μs |
| | | $V_{CC}$=2.7V | 0.25 | — | — | |
| | | $V_{CC}$=5V | 0.25 | — | — | |
| Start condition setup time | $t_{SU.STA}$ | $V_{CC}$=1.8V | 0.6 | — | — | μs |
| | | $V_{CC}$=2.7V | 0.25 | — | — | |
| | | $V_{CC}$=5V | 0.25 | — | — | |
| Data input hold time | $t_{HD.D}$ | $V_{CC}$=1.8V | 0 | — | — | μs |
| | | $V_{CC}$=2.7V | 0 | — | — | |
| | | $V_{CC}$=5V | 0 | — | — | |
| Data input setup time | $t_{SU.D}$ | $V_{CC}$=1.8V | 100 | — | — | ns |
| | | $V_{CC}$=2.7V | 100 | — | — | |
| | | $V_{CC}$=5V | 100 | — | — | |
| Input rise time(2) | $t_R$ | $V_{CC}$=1.8V | — | — | 300 | ns |
| | | $V_{CC}$=2.7V | — | — | 300 | |
| | | $V_{CC}$=5V | — | — | 300 | |
| Input Fall Time(2) | $t_F$ | $V_{CC}$=1.8V | — | — | 300 | ns |
| | | $V_{CC}$=2.7V | — | — | 100 | |
| | | $V_{CC}$=5V | — | — | 100 | |
| Stop condition setup time | $t_{SU.STO}$ | $V_{CC}$=1.8V | 0.6 | — | — | us |
| | | $V_{CC}$=2.7V | 0.25 | — | — | |

| PARAMETER NAME | SYMBOL | TEST CONDITIONS | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| | | $V_{CC}$=5V | 0.25 | — | — | |
| Data output hold time | DH | $V_{CC}$=1.8V | 50 | — | — | ns |
| | | $V_{CC}$=2.7V | 50 | — | — | |
| | | $V_{CC}$=5V | 50 | — | — | |
| WP build time | $t_{SU.WP}$ | $V_{CC}$=1.8V | 1.2 | — | — | us |
| | | $V_{CC}$=2.7V | 0.6 | — | — | |
| | | $V_{CC}$=5V | 0.6 | — | — | |
| WP Keep Time | $t_{HD.WP}$ | $V_{CC}$=1.8V | 1.2 | — | — | us |
| | | $V_{CC}$=2.7V | 0.6 | — | — | |
| | | $V_{CC}$=5V | 0.6 | — | — | |
| Write cycle time | WR | $V_{CC}$=1.8V | — | — | 5 | ms |
| | | $V_{CC}$=2.7V | — | — | 5 | |
| | | $V_{CC}$=5V | — | — | 5 | |
| Page Mode | Durability | $V_{CC}$=5V Tamb=25℃ | 1 million times | — | — | Write cycle |
| | | | 100 years | — | — | Data Retention |

Note: 1. These parameters are characteristic values, not 100% measured values.

# IV. Function Introduction

## 4.1. Device structure

### 4.1.1.Clock data conversion

The SDA pin is typically pulled high by an external device. Data on SDA can only change when SCL is low (as shown in Figure 3). If data changes while SCL is high, it indicates a start or end state.

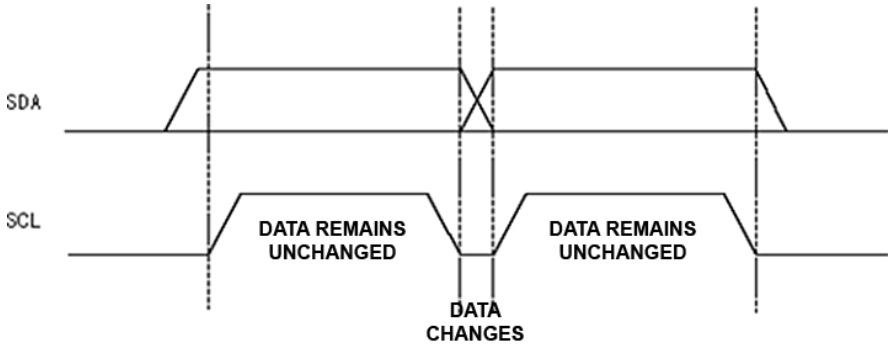


Figure 3. Data valid timing diagram

### 4.1.2. Start (START) state

When SDA transitions from high to low while SCL is high a start condition is generated. The start condition must be generated before all other instructions (as shown in Figure 4).

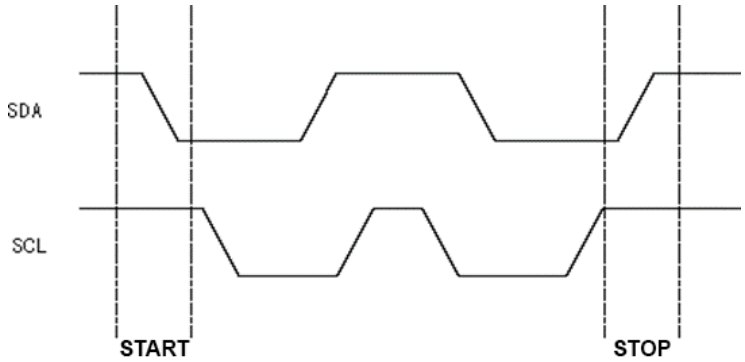


Figure 4. Start and stop timing diagram

### 4.1.3. Stop (STOP) status

When SDA transitions from low to high while SCL is high, a stop condition is generated (as shown in Figure 4). After a series of read operations the STOP command puts the EEPROM into standby mode.

### 4.1.4. ACKNOWLEDGE

After all addresses and data are serially transferred in and out of the EEPROM in 8-bit form, the EEPROM will send a low signal to acknowledge at the ninth clock cycle indicating that it has received each word.

### 4.1.5. STANDBY mode

BST24C512 has a standby mode (standby mode). When it is powered on or receives a stop command and completes internal operations, it will enter the STANDBY mode.

### 4.1.6. Memory reset

After a protocol interruption, power failure, or system reset, the circuit resets as follows: a start condition is established, the clock rises until the ninth cycle, and when SDA is high, a new start condition is created, followed by an end signal. After reset, the device begins new communication.

### 4.1.7.Timing

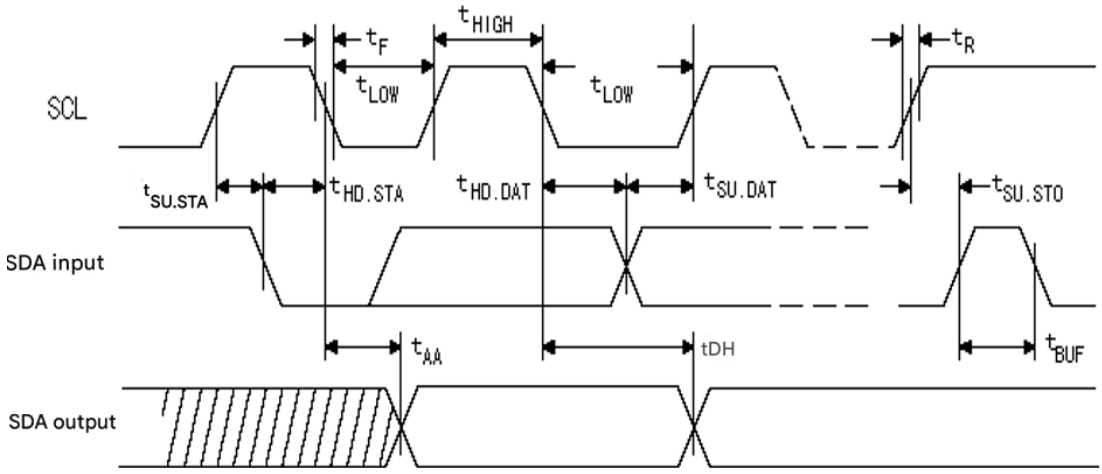


Figure 5. Bus timing

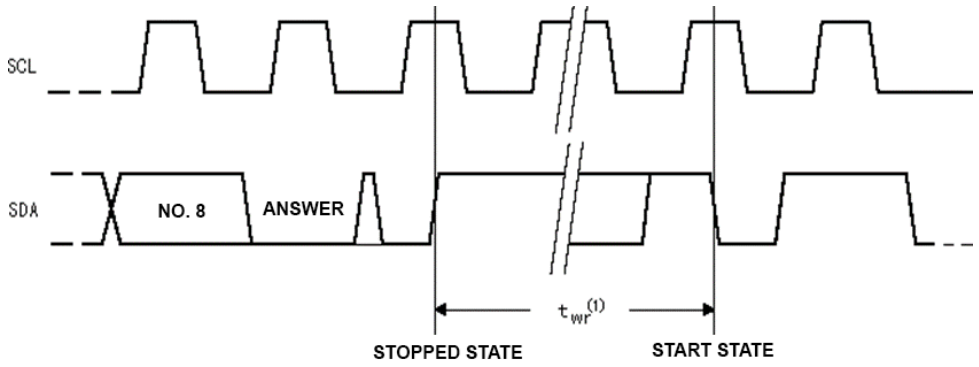


Figure 6. Write cycle timing

Note: 1. Write cycle time twr It is the time from the effective stop state of the write sequence to the end of the internal clear / write cycle

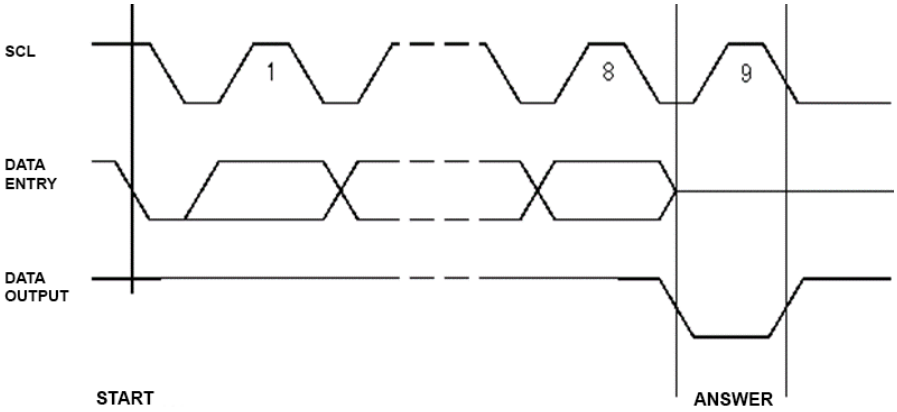


Figure 7. Output response

### 4.2. Device address

After the start state, the BST24C512 EEPROM device requires an 8 -bit device address word to perform a chip read or write operation, as shown in Table 1.

Table 8. Device Address

Highest bit. Lowest bit

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | A2 | A1 | A0 | R/W |

The first four bits of the device address word are fixed at 1010. The next three bits, A2, A1 and A0, are programmable device address bits, allowing up to eight devices on the same bus. These bits must be compared to their corresponding pin hardware-wired inputs. If the A2, A1 and A0 pins are left floating, they are biased to a logic low state using proprietary internal circuitry.

The eighth bit of the device address is the read / write select bit (R /W). A high bit allows a read operation, while a low bit allows a write operation. After comparing the device address, the EEPROM outputs a low level. If the comparison is unsuccessful, the EEPROM enters standby mode.

The data address consists of two 8 - bit data word addresses, as shown in Table 2 and Table 3.

Table 9. First Word Address

Highest bit. Lowest bit

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 |

Table 10. Second word address

Highest bit. Lowest bit

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **B7** | **B6** | **B5** | **B4** | **B3** | **B2** | **B1** | **B0** |

### 4.3. Write operation

#### 4.3.1. Byte Write

The initialization process for a write operation includes the device address, an acknowledge signal, and two 8- bit data word addresses. After receiving the data word address, the EEPROM will send another low-level response, and then the clock will read in the first 8 bits of

data. After all 8 bits of data are received, the EEPROM will send a low -level response. The addressed device (such as a microprocessor) must then send a stop condition signal to terminate the write command. At this point, the EEPROM enters an internally timed write cycle (twr) to write the data to the memory 's physical medium. During the write period, all external inputs are terminated. The EEPROM will not respond again until the data write is complete, as shown in Figure 8.

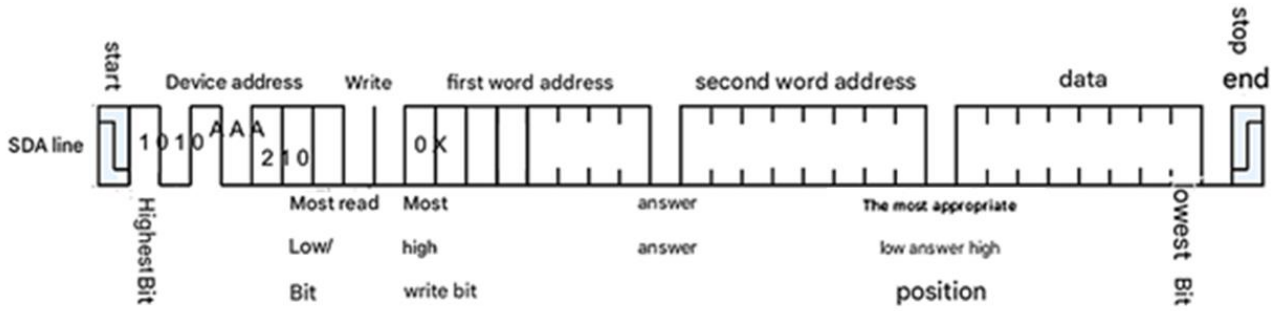


Figure 8. Byte Write

### 4.3.2. Page writing

The BST24C512 's EEPROM uses 128 -bit page writes. The initialization process for a page write is the same as for a byte write. However, after the clock reads the first 8 bits of data, the microprocessor does not send a stop signal. Instead, after the EEPROM receives the 8 bits of data and issues a response, it then transmits the remaining 127 data words. The EEPROM responds with a low level after receiving each data word. The microprocessor must send a stop command to terminate the page write command, as shown in Figure 9.

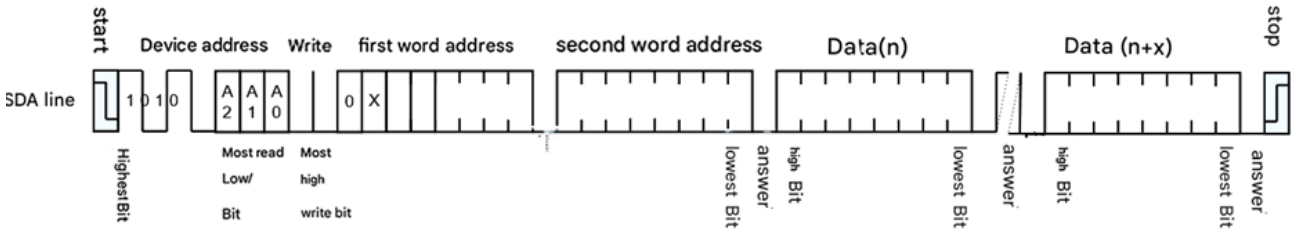


Figure 9. Page Writing

After each data word is received, the lower 7 bits of the data word address are automatically incremented internally. The higher address bits remain unchanged and remain at the row location of the original memory page. When the increment causes the address to reach a page boundary, the next byte is written to the beginning of that page. This means that if more than

128 data words are transferred to the EEPROM data word address will "roll over," overwriting the previous data.

### 4.3.3. Answer poll

Once the internally timed write cycle has been initiated and the EEPROM inputs are disabled, acknowledge polling begins. This involves sending a start signal and the device address word. The read / write bit is the desired operation. Only after the internal write cycle is complete will the EEPROM output a low level as a signal to allow the read or write process to continue.

### 4.3.4. Write identification page

The Identification Page (128 bytes) is an additional page that can be written to and (later) permanently locked in read-only mode. It is written using the Write Identification command. The Write Identification command uses the same protocol and format (format, memory) as the page write command, with the following differences.

- Device type identifier = 1011b ;
- When B10 must be "00", the values of the highest bits B15 and B7 do not matter;

The least significant bitsB6 and B0, define the byte address within the identification page. If the identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (i.e., NOA CK).

### 4.3.5. Lock identification page

The Lock Identification Page command permanently locks the identification page in read-only mode. The Lock Identification Page command is similar to the Write Byte command, with the following specific conditions:

- Device type identifier = 1011b ;
- Address bit B10 must be 1the other address bits do not matter;
- This data byte must be equal to " XXX X XXX 1 X " (X That is, it can be 0 or 1);

## 4.4. Read operation

The initialization process of the read operation is the same as that of the write operation, except that the read / write select bit R/W must be set to 1. The read operation has three modes: current address read, random address read, and sequential address read.

### 4.4.1. Current address read operation

the last read / write operation, the internal data word address counter holds the address of the last operation and automatically increments by one upon completion. This address remains valid during the operation as long as the circuit is powered. Read operations "roll over" the address from the last byte of the last memory page to the first byte of the first page, while write operations "roll over" from the last byte of the current page to the first byte of the same page.

Once the device address and read / write select bit R/ W (to "1") are read in and the EEPROM responds the data word at the current address is read serially. The microprocessor does not generate an input low level response, but instead generates a stop command afterwards, as shown in Figure 10.

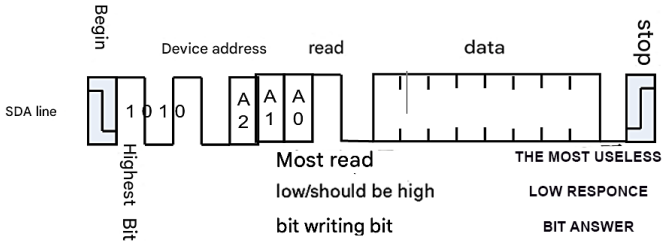


Figure 10. Current address read operation

### 4.4.2. Random address read operation

Random address read operations require a "dummy" byte write operation to load the data word address. Once the device address and data address are read in, the EEPROM responds, the microprocessor must generate a start command. The microprocessor then initializes the address counter by sending a device address (R/W is 1). The EEPROM responds to this device address and reads the data serially. The microprocessor does not respond with a low level, but instead generates a stop command, as shown in Figure 11.

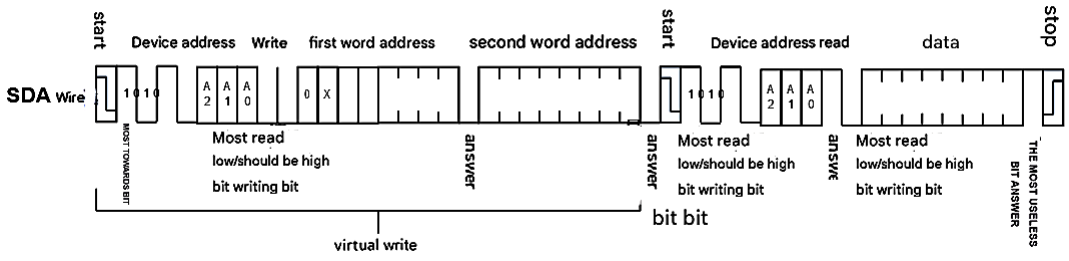


Figure 11. Random address read operation

### 4.4.3. Sequential address read operation

Sequential address read operations can initialize the address counter via a current address read or a random address read. After receiving the data, the microprocessor responds. Once the EEPROM receives this response, the address counter increments by one and the data is read serially. When the maximum address in the memory is reached, the address "rolls over," and the sequential read operation continues. If the microprocessor does not respond with a low level but instead issues a subsequent stop command, the sequential read operation is terminated, as shown in Figure 12.

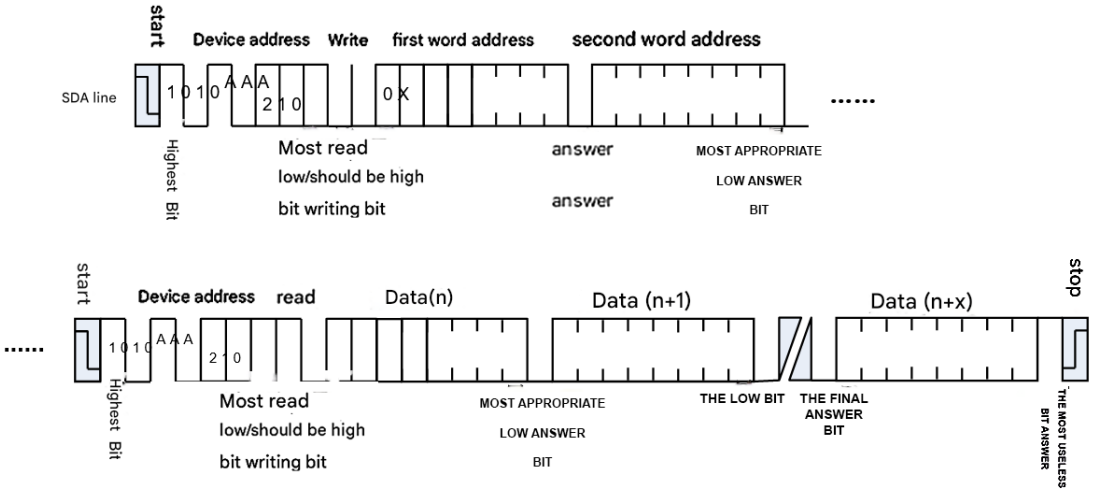


Figure 12. Sequential address read operation

### 4.4.4. Read the identification page

This identification page (128 byte) is an additional page that can be written to and (later) permanently locked in read-only mode. The identification page can be read using the Read Identification instruction, which is defined as 1011b. The read command of the device type identifier uses the same protocol and format. The highest bit B15B7 It doesn't matter, the lowest bit is B6B0 defines the byte address within the identification page. The number of bytes read from the identification page must not exceed the leaf boundary. (For example, when reading the identification page from location 10d. The number of bytes should be less than or equal to 118 because the identification page boundary is 128 byte).

### 4.4.5. Read lock status

/ unlocked status of the identification page can be checked by sending a specific truncation command to the device. If the identification page is not locked, the device returns a response signal, otherwise it returns no response. As shown in Figure 13

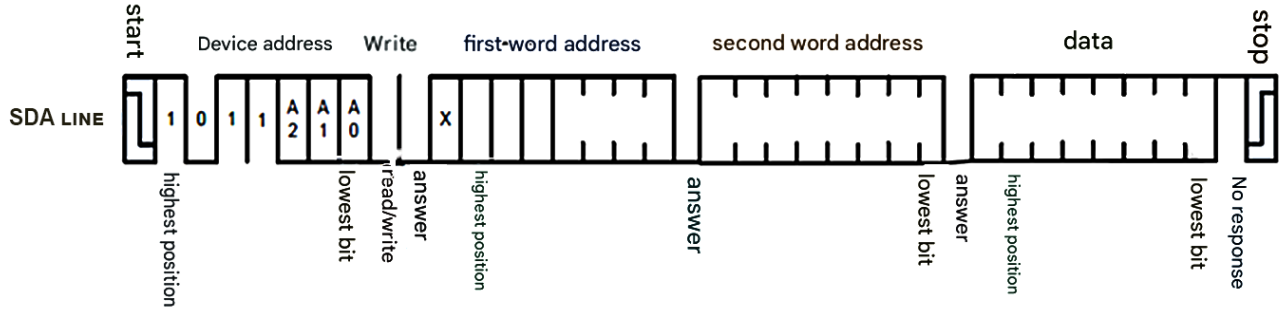


Figure 13. Read latch status

# V. Package size and outline

## 5.1. DIP8 Outline drawing and package dimensions

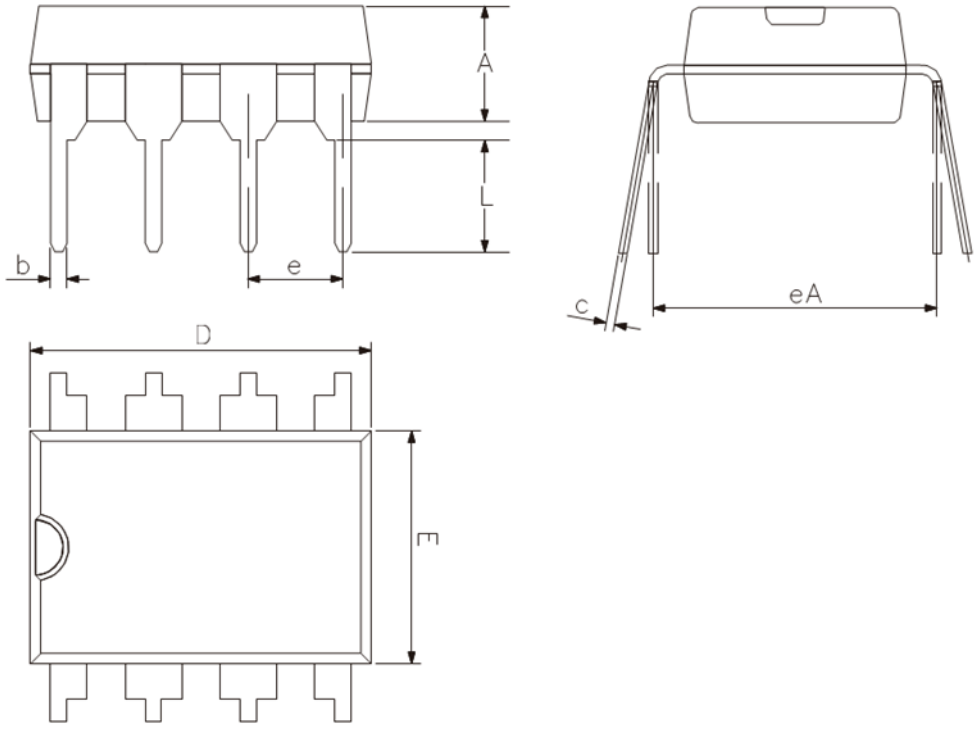


Figure 14.

Table 11.

| 2023/12/A | DIMENSIONS IN MILLIMETERS | |
|---|---|---|
| Symbol | Min | Max |
| A | 3.00 | 3.60 |
| b | 0.36 | 0.56 |
| c | 0.20 | 0.36 |

| | | |
|---|---|---|
| D | 9.00 | 9.45 |
| E | 6.15 | 6.60 |
| e | 2.54 | |
| eA | 7.62 | 9.30 |
| L | 3.00 | — |

## 5.2. SOP8 Outline drawing and package dimensions

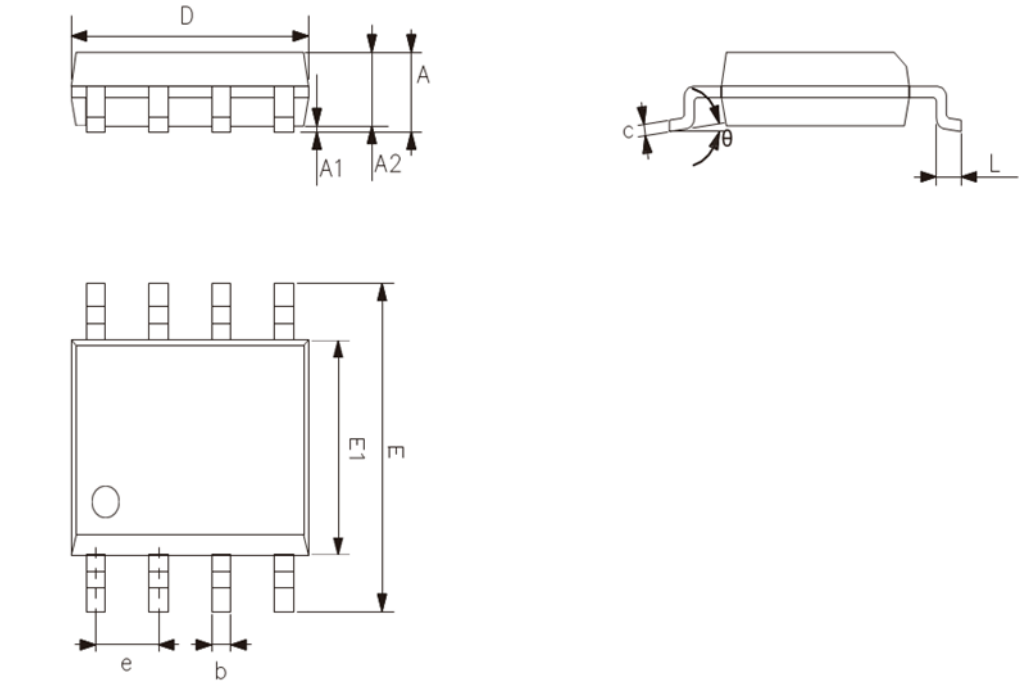


Figure 15.

Table 12.

| 2023/12/A | DIMENSIONS IN MILLIME TERS | |
|---|---|---|
| SYMBOL | MIN | MAX |
| A | 1.35 | 1.80 |
| A1 | 0.05 | 0.25 |
| A2 | 1.25 | 1.55 |
| D | 4.70 | 5.10 |
| E | 5.80 | 6.30 |
| E1 | 3.70 | 4.10 |
| b | 0.306 | 0.51 |
| c | 0.19 | 0.25 |
| e | 1.27 | |
| L | 0.40 | 0.89 |
| θ | 0° | 8° |

## 5.3. TSSOP8 outline drawing and package size

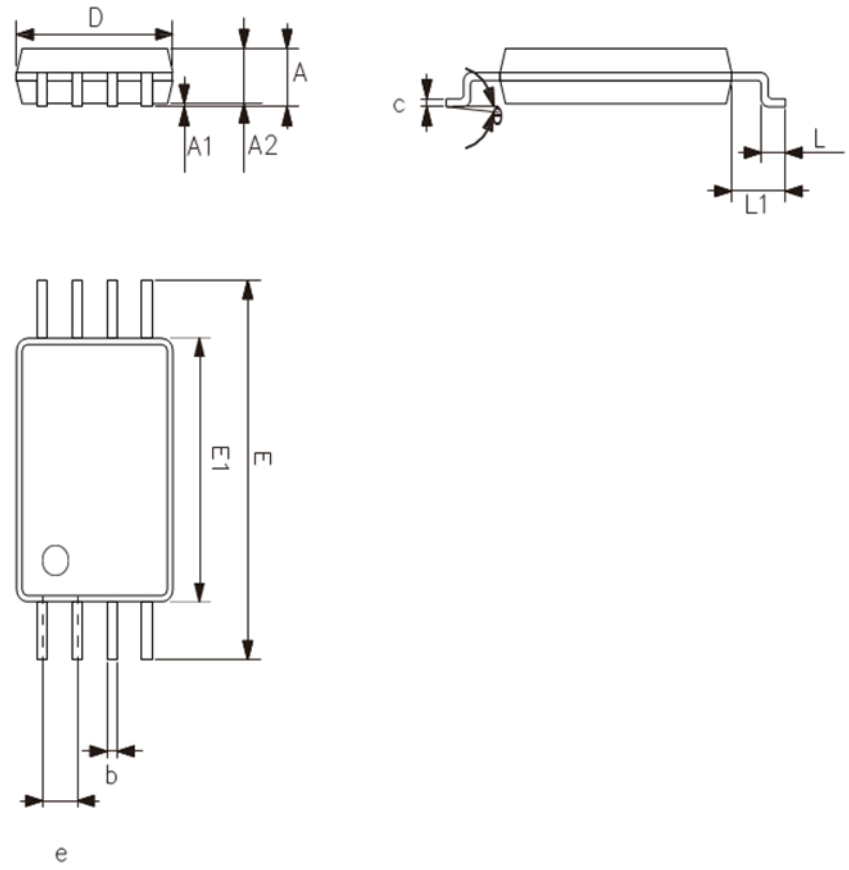


Figure 16.

Table 13.

| 2023/12/A | DIME NSIONS IN MILLIME TERS | |
|---|---|---|
| SYMBOL | MIN | MAX |
| A | — | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 2.90 | 3.10 |
| E1 | 4.30 | 4.50 |
| E | 6.20 | 6.60 |
| e | 0.65 | |
| L | 0.45 | 0.75 |
| L1 | 1.00 | |
| θ | 0° | 8° |

# VI. Statement and Precautions

## 6.1. Content of toxic and hazardous substances or elements in the product

Table 14.

| PART NAME | TOXIC AND HAZARDOUS SUBSTANCES OR ELEMENTS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | LEAD (PB) | MERCURY (HG) | CADMIUM (CD) | HEXACHROMIUM (CR VI) | POLYBROMINATED BIPHENYLS PBBS) | POLYBROMINATED DIPHENYL ETHERS (PBDES) | DIBUTYL PHTHALATE (DBP) | BUTYL BENZYL PHTHALATE (BBP) | DI (2- ETHYLHEXYL) PHTHALATE (DEHP) | DIISOBUTYL PHTHALATE (DIBP) |
| Lead frame | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| Molding resin | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| Chip | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| Inner lead | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| Mounting glue | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| Illustrate | ○：Indicates that the content of the toxic and hazardous substances or elements is in SJ/T11363-2006 below the detection limit of the standard.<br>×: Indicates that the content of the toxic or hazardous substance or element exceeds the limit requirements of SJ/T11363-2006 standard. | | | | | | | | | |

## 6.2. Notice

It is recommended to read this information carefully before using this product;

This information is for reference only. The Company makes no warranties, express or implied, including but not limited to suitability, special applications, or non-infringement of third-party rights.

This product is not intended for use in critical equipment such as life-saving, life-sustaining, or safety-critical equipment, nor is it intended for use in applications where product failure or malfunction could result in personal injury, death, or severe property or environmental damage. Customers using such applications do so at their own risk, and our company assumes no liability for any compensation.

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