

BST24C256 EEPROM

Product Brochure

Rev 7

Revision History

Version	Date	Change Description	Change Person
1	2019-01-09	Initial release	Que Min
2	2019-02-22	Update packaging information and add ordering information	Que Min
3	2019-08-01	Update package information	Que Min
4	2019-09-29	Update standard information	Que Min
5	2022-05-31	Add industrial product ordering information	Que Min
6	2022-06-10	Update the detailed regulation number	Que Min
7	2023-03-09	Updated ESD and CSOP8 ceramic seal dimensions	Que Min

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I. Function

- Fully compatible with I2C protocol
- Memory structure
 - 256Kb (32K bytes)
 - 64 bytes per page
 - Additional write protection
- Working voltage 1.7~5.5V
- Maximum clock frequency: 1 MHz
- Internal Write Cycle
 - AByte write time: 5ms
 - APage write time: 5ms

- Hardware write protection
- Area write protection
- Schmitt trigger suppresses input noise
- High reliability
 - Erase life: 100,000 times
 - Data retention: 20 years
- Enhanced ESD protection
 - HBM 4000V

II. Brief Introduction

- BST24C256 is a serial electrically erasable programmable register (EEPROM) with a capacity of 262144 bits.
- Low power consumption and low voltage, suitable for fields with high power consumption requirements.
- BST24C256 provides an additional 64-byte page area (the Identification Page).

This area can be used to store sensitive data and can be permanently locked.

III. Pin Definition

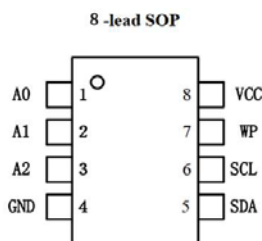


Figure 3-1. Pin Definition

Table 3-1. Pin Function

Pinout	Type	Function
A0-A2	enter	I2C Address
SDA	Input/Output	Serial Data
SCL	enter	Serial clock input
WP	enter	Write protection
GND	Power Ground	land

VCC	power supply	power supply
Sad		

IV. Block Diagram

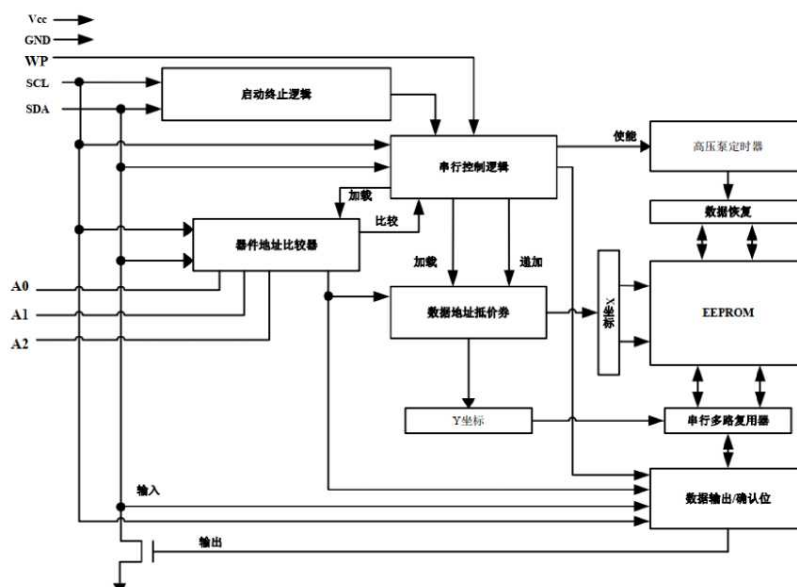


Figure 4-1. Principle block diagram

I2C address (A2, A1 and A0): A2, A1 and A0 are the input pins of the device chip select address. Eight 256K EEPROM devices can be mounted on the same I2C bus at the same time.

SERIAL DATA (SDA): The SDA pin can transmit serial data in both directions. This pin is an open-drain design and can be wired and connected with other open-drain or open-collector devices.

SERIAL CLOCK (SCL): The SCL pin is the clock input, and the SDA pin inputs data on the rising edge of the clock and outputs data on the falling edge.

WRITE PROTECT (WP): BST24C256 provides a write protection pin. When the write protection pin is grounded, the chip data area can be read and written; when the write protection pin is connected to the power supply, the data area write protection is effective. The pin functions are shown in the table below.

Table 4-1. WP pin function

WP Pins	Function
Connect to VCC	Data area protection

Connect to GND	Normal read/write
----------------	-------------------

V. Functional Description

5.1. Memory structure

BST24C256: The memory structure is 512 pages, each page is 64 bytes, and requires 15 data address bits.

B15	B14		B13	B12	B11	B10	B9	B8
-----	-----	--	-----	-----	-----	-----	----	----

Figure 5-1. Data address high 8 bits (MSB)

	B6	B5	B4	B3	B2	B1	B0
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Figure 5-2. Data address lower 8 bits (LSB)

5.2. Device Operation

5.2.1. Clock and Data

Usually the SDA pin needs to be pulled up when connected to other devices. During data transmission, the SDA level is allowed to change only when SCL is low. [\(Figure 5-3\)](#) When SCL is high, the falling edge of SDA is called the start condition, and the rising edge is called the stop condition. [\(Figure 5-4\)](#) The start condition must be issued before other instructions, and the stop condition causes the EEPROM to enter a low-power standby mode.

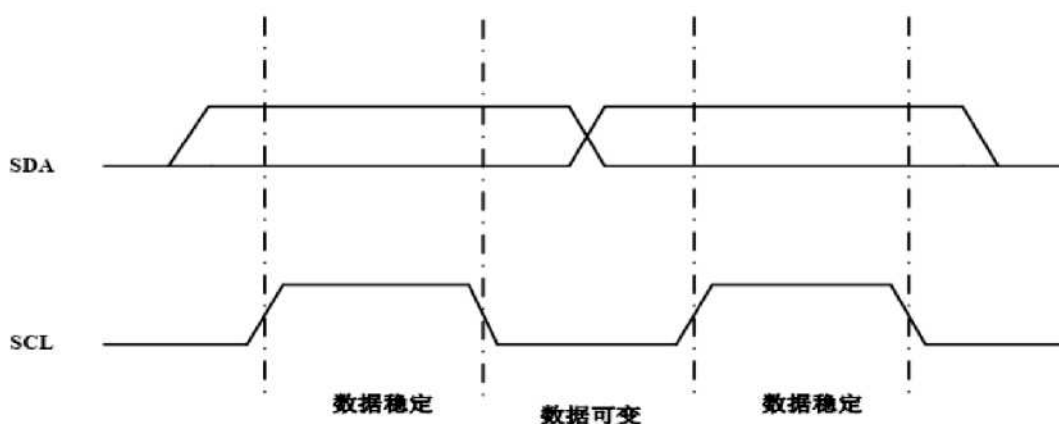


Figure 5-3. Valid data

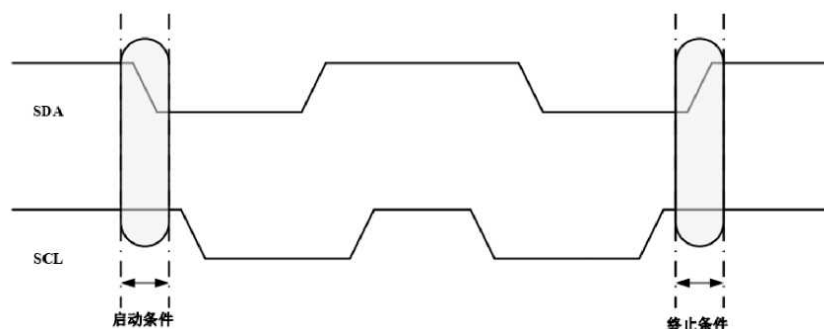


Figure 5-4. Start condition and end condition

5.2.2. Answer

The receiver on the I2C bus sends a "0" in the ninth clock cycle every time it receives 8 bits of data, generating an acknowledgement signal to indicate that the 8-bit data transmission is successful. The transmitter on the I2C bus, whether it is a master device or a slave device, must release SDA after sending 8 bits of data. In the ninth clock pulse cycle, the receiver pulls SDA low, indicating that the 8-bit data information is successfully received.

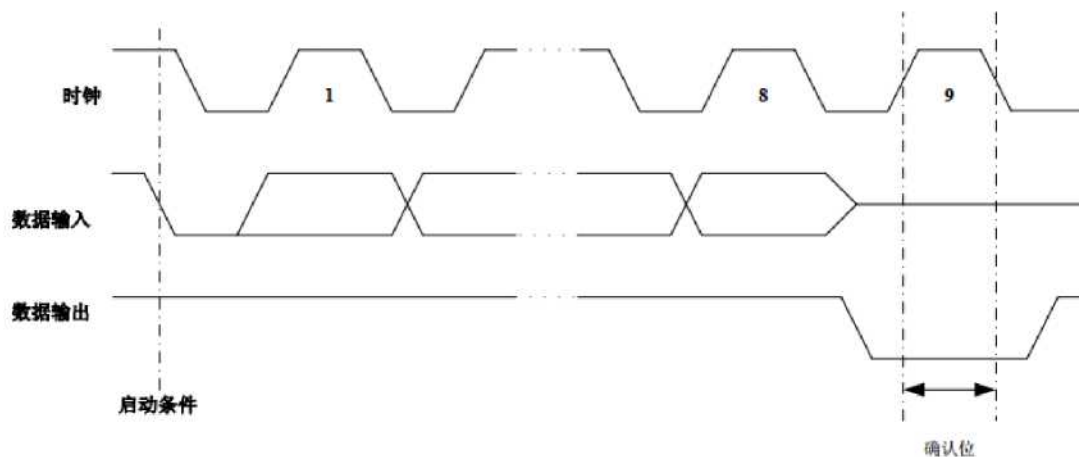


Figure 5-5. Response

5.2.3. Standby mode

There are two situations that can make BST24C256 enter low power standby mode:

- After power-on to before the first instruction is issued;
- Receive the termination condition instruction and complete the internal operation;

5.2.4. Restart

After the transmission protocol is interrupted, power is lost or the system is reset, the EEPROM can be restarted in the following ways:

- In a maximum of 9 clock cycles, when SDA is "1", a start condition instruction is successfully sent;
- 2, or send 9 start condition instructions continuously.

5.2.5 Write protection

When the WP pin of BST24C256 is connected to VCC, the hardware write protection is effective and the entire EEPROM can only be read.

5.3. Device Address

EEPROM requires an 8-bit address word to specify the device address of the EEPROM. The first 4 bits of the 8-bit address word are fixed to 1010. The next 3 bits are the device address bits, corresponding to the levels of the device's A2, A1 and A0 pins; the last bit is the read/write flag, "1" for read operation and "0" for write operation.

MSBLSB

1	0	1	0	A2	A1	A0	R/W
---	---	---	---	----	----	----	-----

Figure 5-6. Device address

After the EEPROM receives the start signal and the EEPROM address information, if the address bit in the address information matches the chip select of the EEPROM, the EEPROM returns a response signal. If the address bit and the chip select do not match, the EEPROM will enter the standby mode.

5.4. Write Operation

5.4.1. Byte Write Operation

In the byte write operation mode, the master device sends a start signal and address information to the EEPROM, then sends two 8-bit data addresses, and then sends 8-bit data. After receiving each 8-bit data address or data, the EEPROM returns an acknowledge signal. After the master device completes the transmission, it sends a termination signal, and the EEPROM starts the internal erase process (tWR). During the internal erase process, the EEPROM no longer responds to any request from the master device. [\(Figure 5-7\).](#)

5.4.2. Page Write Operation

In the page write operation mode, up to 64 bytes of data can be written at a time. The page write operation is similar to the byte write operation, except that the master device continuously sends up to 64 bytes of data. Every time 8 bits of data are received, the lower 6 bits of the EEPROM internal address register are automatically increased by 1, and the higher bits remain unchanged. When the master device continuously sends more than 64 bytes of data, the lower 6 bits of the EEPROM internal address register will roll back to the starting state, and the previous data will be overwritten. When all 64 bytes of data are sent, the master device sends a termination signal, and the EEPROM starts the internal write operation, and all data is written in one write cycle. During the internal erase process, the EEPROM no longer responds to any requests from the master device.

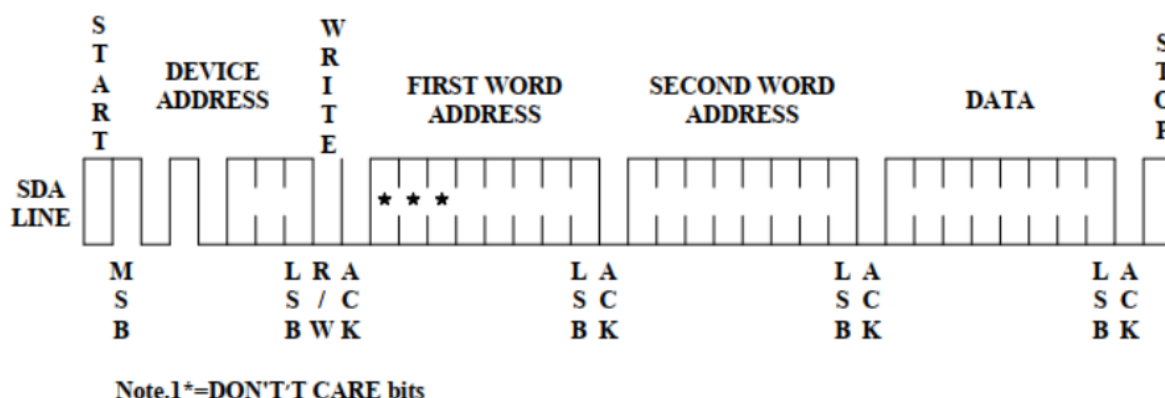


Figure 5-7. Byte Write

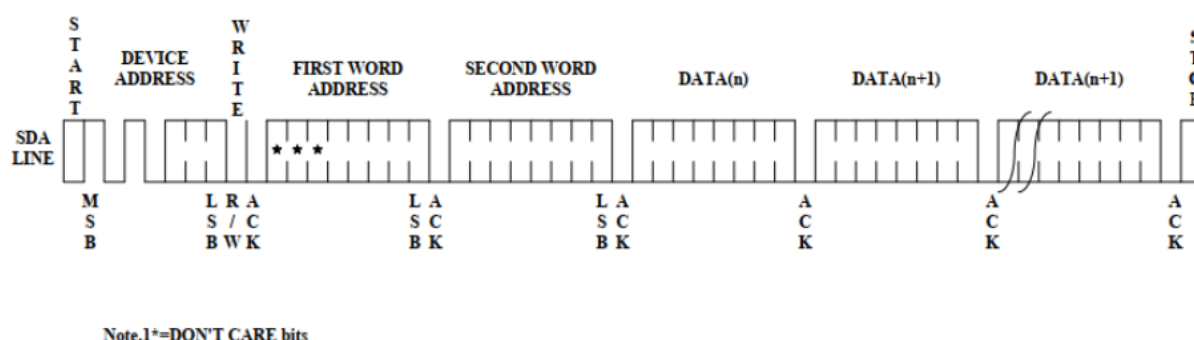


Figure 5-8. Page Writing

5.4.3. ID Page Write Operation

The EEPROM has an additional 64-byte ID page that can be set as a permanent write in subsequent operations

Protected mode. The write operation of the ID page is similar to the normal page write operation, with the following differences:

- Device Type Definition = 1011b.
- In the MSB address, B15 - B6 can be any value, and B10 must be "0".
- The LSB address B5 - B0 defines the address of each byte in the ID page.

When the ID page is locked, the ID page cannot be written. The EEPROM does not return a response signal to the ID page write command.

Number.

5.4.4. Poll Response

When the EEPROM enters the internal write cycle, the EEPROM does not respond to any external commands. At this time, the master device can use polling to send a start signal and address. When the EEPROM internal write operation is completed, a response signal will be returned to inform the master device that the next read and write operation can be performed.

5.5. Read Operation

The read operation is similar to the write operation, just set the read/write bit to "1". There are three modes of read operation: current address read, random address read and continuous read.

5.5.1. Current address read operation

When the device is not powered off, the internal address register saves the address of the last read or write operation and adds 1. If the previous read/write operation points to address N, then the data at address N+1 is read. If N is the last byte of the storage unit, then the first byte of the first page is read. When the read instruction containing the device address information is sent with the clock, the EEPROM returns an acknowledge signal and then outputs 8 bits of data. The master device does not send an acknowledge signal, but must output a termination signal to terminate the current address. Address read operation.

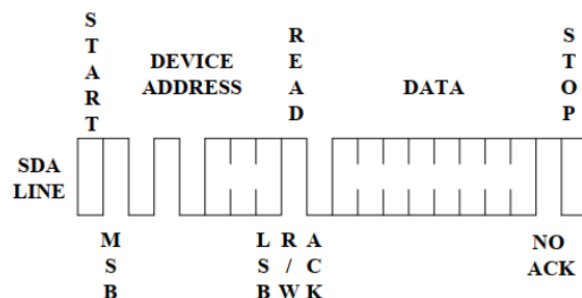


Figure 5-9. Current address read error! Reference source not found.

5.5.2. Random address read operation

The random read operation allows the master to read any byte of the EEPROM. The master first performs a dummy write operation by sending a start signal and the EEPROM I2C address and the address of the byte data it wants to read. After the EEPROM responds, the master resends the start signal and the EEPROM device address.

At this time, the R/W position is set to "1". The EEPROM responds and sends an acknowledge signal, and then outputs the required 8-bit byte data. The master device does not send an acknowledge signal, but must generate a termination signal to terminate the read operation.

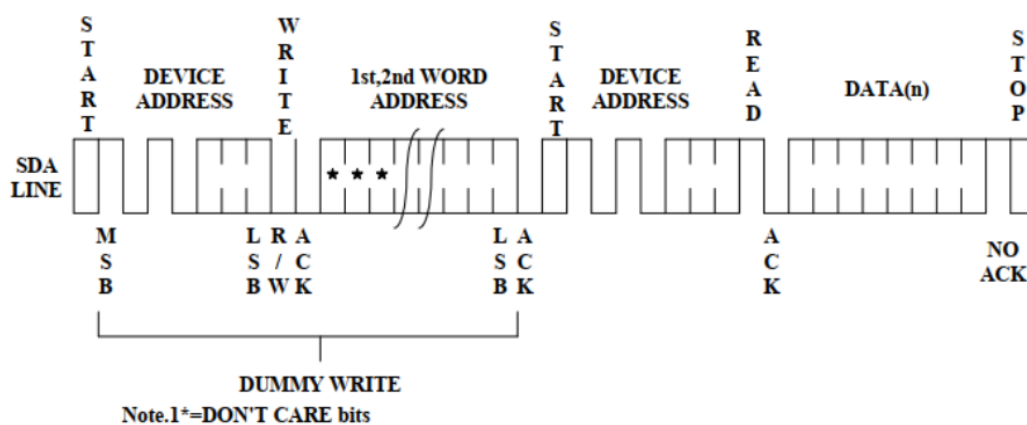


Figure 5-10. Random address read

5.5.3. Continuous read operation

The continuous read operation can be started by the current address read operation or the random address read operation. When the master device receives the first data, it sends an acknowledgement signal. When the EEPROM receives this acknowledgement signal, the internal address register is incremented by 1 and continues to output 8 bits of data. When the data address reaches the last position of the storage unit, the data address will roll back and continue to output data from the first address of the storage unit. The continuous read operation ends when the master device sends a stop command, and there is no need to send an acknowledgement command.

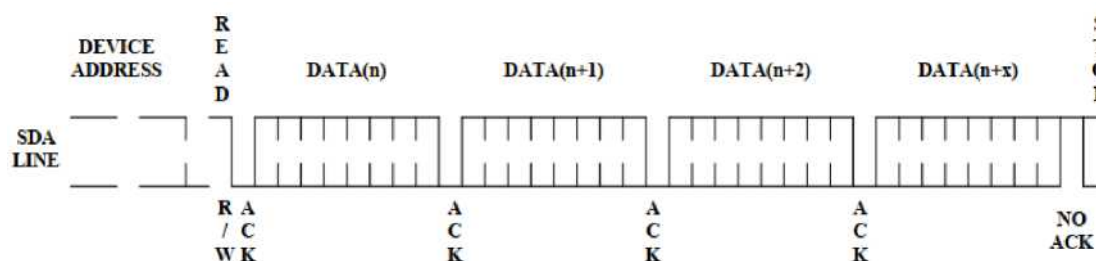


Figure 5-11. Continuous Read

5.5.4. Read ID page operation

The instruction to read the ID page is similar to the random address read instruction, the only difference is

- Device Type Definition = 1011b.
- In the MSB address, B15 - B6 can be any value, and B10 must be "1".
- The LSB address B5 - B0 defines the address of each byte in the ID page.
- The data bytes read by the read ID page instruction cannot exceed the boundary of the ID page (for example, when reading the ID page address

When it is 0xA, the number of data read cannot exceed 54bytes, because the ID page has a total of 64 bytes).

5.5.5. ID page write protection

The ID page write protection instruction sets the ID page to permanent read-only mode. It is similar to the byte write instruction, with the following differences:

- Device Type Definition = 1011b.
- B10 in the MSB address must be "1", other values are arbitrary.
- Write data to "XXXXXX1X", x is any value.

VI. Electrical characteristics

Maximum Ratings:

- DC power supply voltage: -0.3V ~ +6.5V
- DC input/output voltage: GND-0.3V ~ VCC+0.3V
- Operating temperature: -55°C ~ +125°C
- Storage temperature: -65°C ~ +150°C
- Antistatic voltage (human body model): 4000V

Notice:

Working beyond the maximum rated parameters may cause permanent damage to the device. When the maximum rated parameters are exceeded, the device performance may not reach the expected performance. Working beyond the maximum rated parameters for a long time may affect the reliability of the device.

6.1. DC electrical characteristics

Operating conditions TA = -55°C to +125°C, VCC = +1.7V to +5.5V (unless otherwise specified)

Table 6-1. DC electrical characteristics

Parameter	Symbol	Test conditions	Minimum	Maximum	Unit
Working power supply current	Icc1	Vcc=5.0V Read @400kHz	-	5	mA
Standby power current	I _{sb} 1	Vcc=5.0V Vin=Vcc or Vss	-	50	μA
Input leakage current	I _{li}	Vcc=5.5V Vin=Vcc or Vss	-	10	μA

Output leakage current	I _{lo}	V _{cc} =5.5V V _{out} =V _{cc} or V _{ss}	-	100	μA
Input low level voltage	V _{il1}	V _{cc} =3.3V	-	V _{cc} ×0.2	V
Input high level voltage	V _{ih1}	V _{cc} =3.3V	V _{cc} ×0.7	-	V
Output low level voltage	V _{ol1}	V _{cc} =1.7V	-	0.2	V

Parameter	Symbol	Test conditions	Minimum	Maximum	Unit
		I _{ol} =0.15mA			
Output low level voltage	V _{ol2}	V _{CC} =5.0V I _{ol} =3.0mA	-	0.4	V

6.2. AC electrical characteristics

Operating conditions TA = -55°C to +125°C, VCC = +1.7V to +5.5V, CL = 100 pF (unless otherwise specified)

Table 6-2. AC electrical characteristics

Parameter	Symbol	1.7V≤VCC < 2.5V		2.5V≤VCC < 5.5V		Unit
		Minimum	Maximum	Minimum	Maximum	
Clock frequency	f _{cl}	-	400	-	1000	KHz
Clock low level width	t _{low}	0.6	-	0.6	-	μs
Clock high level width	t _{high}	0.4	-	0.4	-	μs
The interval time from the falling edge of the clock to the valid output of data	t _{aa}	-	0.9	-	0.9	μs
Bus release time	t _{buf}	0.5	-	0.5	-	μs
Start condition hold time	t _{hd:sta}	0.35	-	0.35	-	μs
Start condition setup time	t _{su:sta}	0.35	-	0.35	-	μs
Data input hold time	t _{hd:dat}	0	-	0	-	μs
Data input setup time	t _{su:dat}	200	-	200	-	ns
Input rise time	t _r	-	0.3	-	0.3	μs
Input Fall Time	t _f	-	0.3	-	0.3	μs
Termination condition establishment time	t _{su:sto}	0.25	-	0.25	-	μs
Data output hold time	t _d	50	-	50	-	ns
Write cycle	t _w	-	5	-	5	ms

VII. Timing

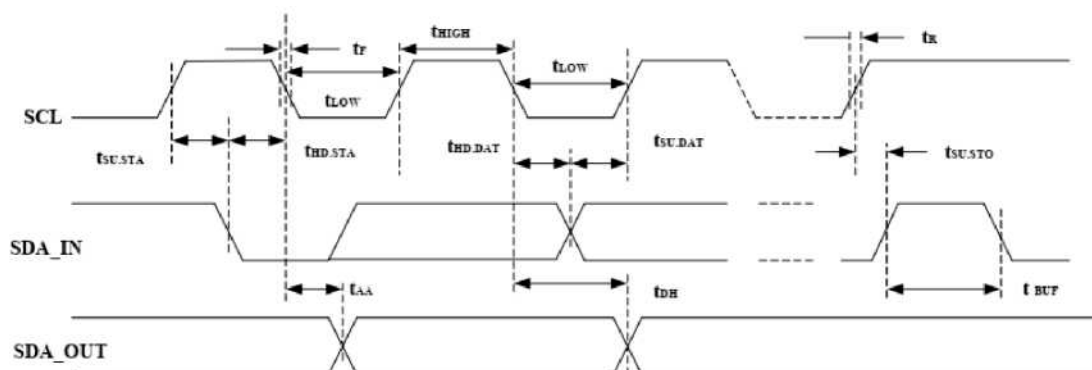


Figure 7-1. Bus timing

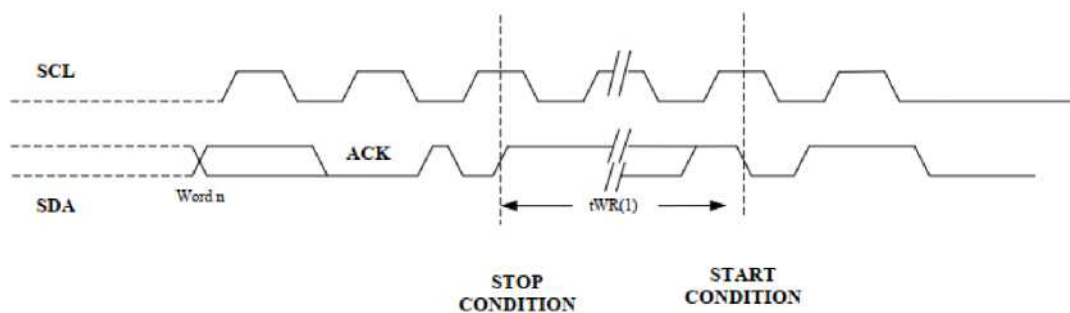


Figure 7-2. Write cycle timing

Note:

The write cycle (t_{WR}) is the time period from the termination condition in a legal write instruction to the completion of the internal write of the device.

VIII. Packaging

8.1. SOP8

SOP8 plastic package dimensions are as follows:

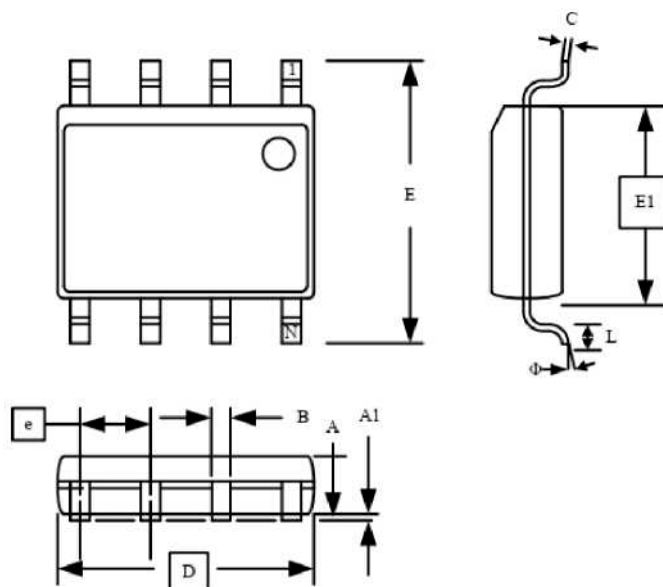


Figure 8-1. SOP8 package dimensions

Table 8-1. SOP8 dimensions

Dimension symbols	Value (unit: mm)		
	Minimum	Nominal	Maximum
A	1.35	—	1.75
A1	0.10	—	0.25
B	0.31	—	0.51
C	0.17	—	0.26
D	4.70	—	5.10
E1	3.70	—	4.10
E	5.70	—	6.20
e	—	1.27	—
L	0.40	—	1.30

Φ	0°	—	8°
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8.2. CSOP8

The dimensions of CSOP8 ceramic seal are as follows:

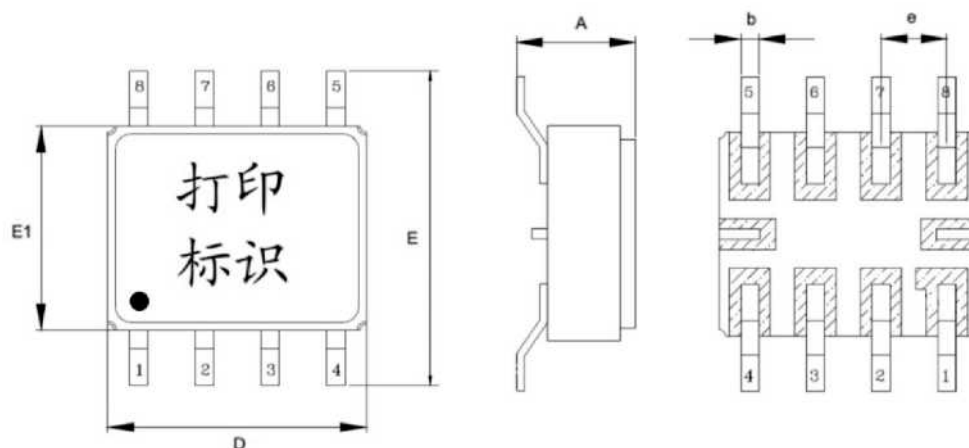


Figure 8-2. CSOP8 package dimensions

Table 8-2. CSOP8 dimensions

Dimension symbols	Value (unit: mm)		
	Minimum	Nominal	Maximum
A	-	-	2.7
b	0.28	-	0.42
D	4.7	-	5.3
E1	3.6	-	4.2
E	5.7	-	6.3
e	-	1.27	-

IX. Ordering Information

Table 9-1. Product ordering information

Model	Package Name	Quality Grade	Detailed regulation number
BST24C256ESOP8	SOP8	Military Temperature	Q/BST 20416-2018
BST24C256MCSOP8	CSOP8	B	Q/BST 20501-2019
BST24C256-A	SOP8	Industrial Grade	Q/BST 50061-2021