BST18V04 series high speed PROM

Product Brochure

Revision History

Serial number	Edition	Change Description	Change order number	Change Person	Change Date	Remark
1	1.0	Initial release	NA	Hou Kejun	2019/11/24	
2	2.0	• Change to series product manual; • Add product ordering information; • Optimize the format • The company name was changed to "Limited Liability Company" • 5. Improve the CQFP44 package dimensions (increase Lp value)	NA	Tu Yikun	2021.11.25	
3	2.1	Corrected the CQFP44 package dimensions to be consistent with the detailed specifications	NA	Tu Yikun	2021.12.7	

I. Order record

- Product use and application scope
- Standards
  - General specifications
  - Testing agency and test report number
- Product features
  - Product features

- Product appearance, structure, assembly and usage characteristics
  - Product structure
  - Product features
- Product materials and processes
  - Process structure
  - Lead materials and coatings
- appearance and pictures of the actual product
  - Product appearance
  - Product pictures
- Terminal arrangement
- performance indicators
  - Absolute maximum ratings
  - Recommended operating conditions
  - Electrical characteristics
- Typical application circuit diagram
  - BST8v configuration fpga connection
  - Fpga master serial mode overview
  - Cascade configuration overview
- Initialize fpga configuration
- Select configuration mode
- How to use mb mode

- Configuring storage requirements
- operating procedures and precautions
- Product ordering information
- R&d and production units
- Appendix
- Csmt jtag programmer user manual
- Mcssvf software usage instructions

II. Product use and application range

BST18V04 series is a military-grade 3.3V rewritable PROM. The memory size is 4Mbit. Its normal mode is 4Mbits capacity, which can be expanded to 8Mbits through special instructions. It is compatible with IEEE1532 in-system programming standard and can be programmed in the system using JTAG port. Flash can be programmed and configured in the system working environment. Under the full temperature system range working requirements, a large amount of FPGA configuration data stream is stored in a reliable non-volatile manner.

When the FPGA works in the master serial mode, the FPGA provides a clock CCLK (configuration clock) to drive the BST18V04MCQFP44. A short time after the rising edge of CCLK, the data on the D0 pin of the PROM (which is connected to Din on the FPGA) is valid, and the FPGA generates appropriate clock pulses to complete the configuration. When the FPGA works in the slave serial mode, the clocks of the PROM and FPGA are both provided externally.

When the FPGA works in SelectMAP mode (Slave), the external crystal oscillator

generates a clock to drive the PROM and FPGA. At the rising edge of the clock, the data of D[7:0] of the PROM is valid, and at the next rising edge of the clock, the data will be latched into the FPGA.

By driving the CE of the second PROM through the CEO output, we can support multiple PROMs to be used together to increase storage capacity. The clocks and data of these PROMs are connected together, and these PROMs can be coordinated with other types of PROMs.

2.1. General Specifications

GB/7092-1993 Dimensions of semiconductor integrated circuits

GB/T17574-1998 Semiconductor device integrated circuits

GJB548B-2005 Microelectronic Device Test Methods and Procedures

GJB97B-2012 General Specification for Semiconductor Integrated Circuits

GJB7400-2011 General specification for semiconductor integrated circuits for use in qualified manufacturer certification

III. Product Features

3.1 Product Features

This device is a high-performance PROM chip with advanced in-system programming and

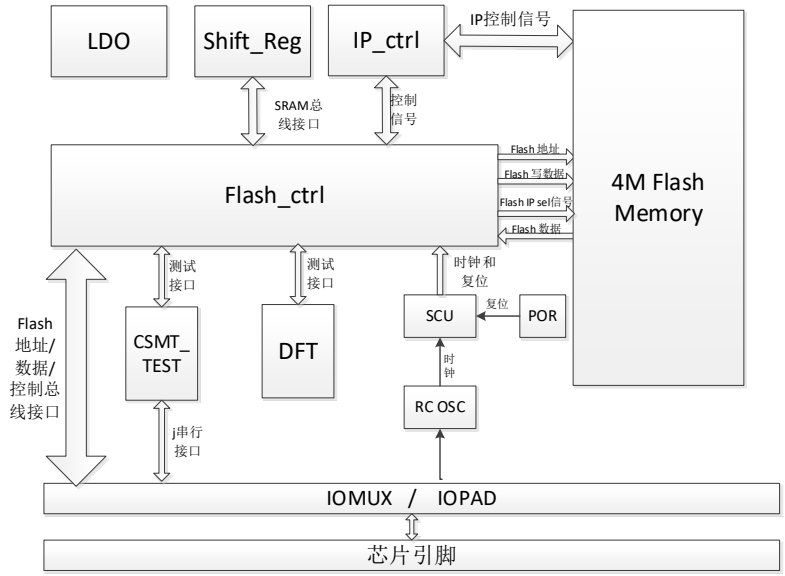
testing capabilities. Its normal mode has a capacity of 4Mbits, which can be expanded to 8Mbits through special instructions. It is compatible with the IEEE1532 in-system programming standard and can be programmed in-system using the JTAG port. At the same time, the chip has encryption and configuration serial parallel output functions. The chip's maximum operating frequency is 33MHz. The replacement product information is as follows:

Our Products	Alternative Products	Alternative Products Company	Alternative product country
BST18V04	XQ18V04	Xilinx	USA

3.2. Features of product appearance, structure, assembly and use

3.2.1. Product Structure

BST18V04MCQFP44The overall architecture is shown in the figure below:



Picture 1. Functional module diagram

3.2.2. Product Features

- Normal operating temperature range: –55°C~ +125°C
- Low-power programmable BSTOS memory can effectively suppress static noise interference
- FPGAs normally operate with a power supply voltage of 3.3V
- Provides 10,000 programmable/erasable cycles
- Compliant with IEEE Std 1149.1 boundary scan (JTAG) standard
- Two configuration modes:
- Slow/Fast serial configuration modes, up to 20 MHz
- Parallel configuration mode data transmission speed reaches 160Mbps at 20Mhz
- The maximum I/O voltage is 5V, and both 3.3V and 2.5V signals are allowed to be input and output.
- The output voltage has 3.3V and 2.5V drive capability
- The chip package is CQFP-44
- Support Xilinx ISE software (in 8Mb mode, it is necessary to use Chengdu Huawei's self-developed software)

IV. Product materials and processes

4.1. Process structure

The circuit is 90nm, BSTOS process, circuit scale number is 40Ten thousandNumber of doors.

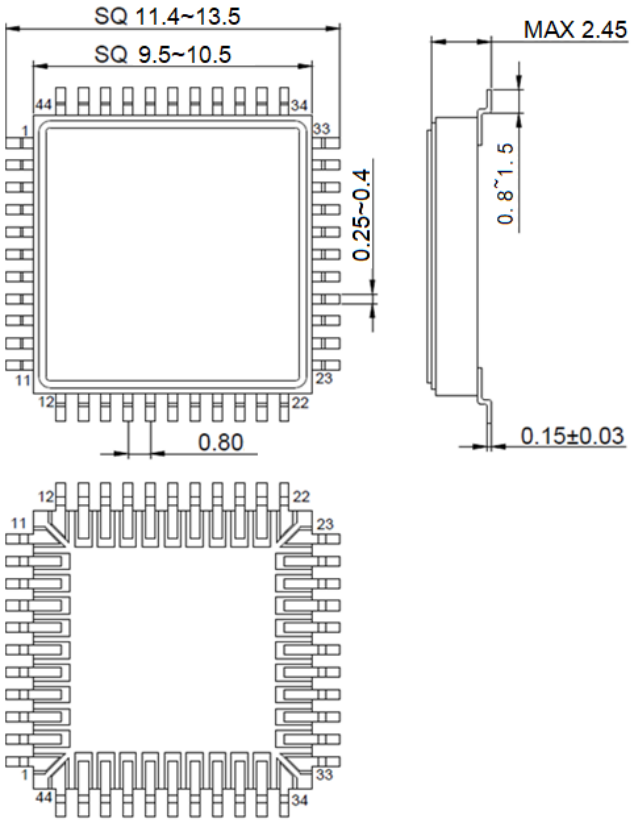
4.2. Lead Materials and Coatings

Lead wire material should be in accordance with GJB 597B-The provisions of 3.5.7 of 2012.Lead material is Kovar alloy, nickel-plated and gold-plated.

V. Appearance and pictures

5.1.Product appearance

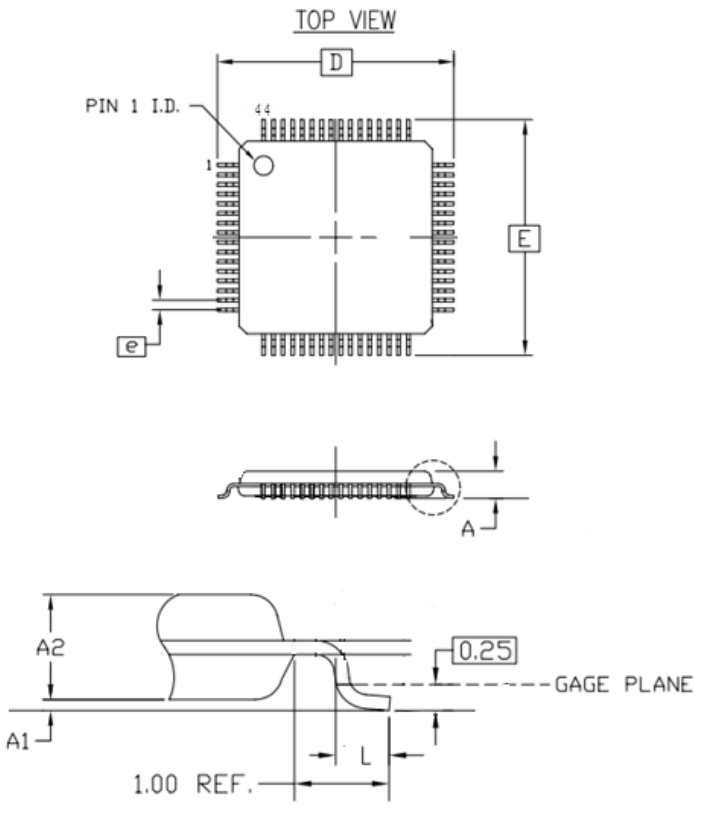
The CQFP44 package dimensions refer to the provisions of GB/T 7092-1993, and the appearance is shown below.



Unit is mm

Picture 2. CQFP44 Dimensions

The TQFP44 package dimensions refer to the provisions of GB/T 7092-1993, and the appearance is shown below.



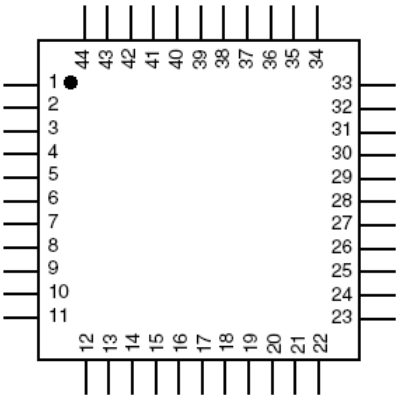
尺寸 符号	数值		
	最小	公称	最大
A	—	—	1.6
A1	0.05	—	0.15
A2	1.35	1.4	1.45
D	11.8	12	12.2
E	11.8	12	12.2
D1	9.9	10	10.1
E1	9.9	10	10.1
b	0.28	—	0.36
e	—	0.8	—
L	0.45	—	0.75

Unit is mm

Picture 3. TQFP44 Dimensions

VI. Terminal arrangement

The lead-out terminals shall be arranged as shown in Figure 4 (top view).



Picture 4. Package Pinout Top View

Table 1. Package pin definition

Pin number	Symbol	Achievement able	Pin number	Symbol	Achievement able
1	NC	Floating pin	23	NC	Floating pin
2	NC	Floating pin	24	NC	Floating pin
3	TID	JTAGTest data input	25	D5	Parallel data output D5 bit
4	NC	Floating pin	26	VCCO	IO Power
5	TMS	JTAGTest Mode	27	D3	Parallel data outputD3-digit
6	GND	land	28	GND	land
7	TCK	JTAGTest Clock	29	D1	Parallel data output D1 bit
8	VCCO	IO Power	30	NC	Floating pin
9	D4	Parallel data output D4 bit	31	TDO	JTAGTest data output
10	/CF	Configuring Signals	32	NC	Floating pin
11	NC	Floating pin	33	NC	Floating pin
12	NC	Floating pin	34	NC	Floating pin
13	OE/RESET	Output enable signal/ Reset signal	35	VCCINT	Internal logic power supply
14	D6	Parallel data output D bit	36	VCCO	IO Power
15	/CE	Enable signal	37	NC	Floating pin
16	VCCO	IO Power	38	VCCINT	Internal logic power supply

Pin number	Symbol	Achievement able	Pin number	Symbol	Achievement able
17	VCCINT	Internal logic power supply	39	NC	Floating pin
18	GND	land	40	D0	Data output D0 bit
19	D7	Parallel data output D7 bit	41	GND	land
20	NC	Floating pin	42	D2	Parallel data output D2 bit
21	/CEO	Chip enable output signal	43	CLK	Clock signal
22	NC	Floating pin	44	NC	Floating pin

VII. Performance Indicators

7.1. Absolute Maximum Ratings

Power supply voltage -0.5V～4.0V

DC input voltage to ground (VIN) -0.5V～3.6V

Three-state output voltage to ground (VTS) -0.5V～3.6V

Power consumption (PD) 100mW

Storage temperature (Tstg) -65℃～+150℃

Maximum soldering temperature (Th) 300℃ (10s)

Junction temperature (TJ) 175℃

7.2. Recommended operating conditions

Power supply voltage (VCCINT/VCCO) 3.0V～3.6V

Low level input voltage (VIL) 0V～0.8V

High level input voltage (VIH) 2.0V～VCCO

Working environment temperature (TA) -55℃～125℃

7.3. Electrical properties

Unless otherwise specified, the electrical characteristics shall be as specified in Table 3 and shall be applicable to the full operating temperature range of -55℃≤TA≤125℃ and tested with reference to GB/T 17574-1998.

Table 2. Electrical characteristics

Characteristic	Symbol	Condition Unless otherwise specified VCCINT = CCO= 3.3V -55℃≤TA≤125℃	Limit value		unit
			Minimum	Maximum	
Output high level voltage	VOH	IOH=-4.0mA	2.5	—	V
Output low level voltage	VOL	IOL=4mA	—	0.45	V
Maximum output drive current	IOL	—	4	—	mA
Input high level voltage	VIH		2.0	—	V
Input low level voltage	VIL		—	0.8	V
Input leakage current	II	VIN=GNDorVCCO	-20	+20	μA
Output high impedance leakage current	IOZ	VIN=GNDorVCCO	-20	+20	μA
Supply Current	ICC	Without load, f=1MHz	—	25	mA
OE/RESET_ to data output delay	T8h	f=1MHz	—	20	ns
CE_ to data output delay	tCE	f=1MHz	—	20	ns

CLK to data output delay	tCO	f=1MHz	—	30	ns
Maximum operating frequency	f		33	—	MHz
Functional testing		Supply voltage=3.3V,Perform functional tests according to the prepared test procedures.	—		

VIII. Typical application circuit diagram

8.1. BST18V04 FPGA configuration connection

- The DATA output of BST18V04 drives the Din terminal of the main FPGA chip;
- The output of the master FPGA CCLK drives the BST18V04 at the CLK end (in master serial and master parallel modes);
- In daisy-chain mode, the CEO output of the BST18V04 drives the CE terminal of the next BST18V04;
- The RESET input of the BST18V04 is preferably driven by the INIT pin of the main FPGA chip. This connection ensures that the internal address counter of the BST 18V04 is reset before configuration in any case, even in the case described above due to a Vcc glitch.
- If the DONE terminal of the main FPGA chip is not constantly grounded, the CE input terminal of the first BST 18V04 (or the only BST18V04) in the daisy chain can be driven by the DONE output terminal of the main FPGA chip. The CE terminal of the BST18V04 can also be constantly set to a low level. This operation method will make the data output always valid and will generate an unnecessary current of up to 20mA.

- In serial configuration mode, D1-D7 pins will be in high impedance state, and D1-D7 can be left floating.
- SelectMap mode is similar to slave parallel configuration mode. The frequency of data is to send one BYTE of data per CCLK instead of one BIT of data per CCLK. Please refer to the FPGA data sheet for specific configuration requirements.

8.2. FPGA Master Serial Mode Overview

The FPGA's configurable logic block (CLB) I/O, logic blocks, and their interconnections are determined by the configuration program. The board automatically completes program loading during power-on, and can also be determined by the state of the three mode pins of the instruction-FPGA. In the main string mode, the FPGA automatically loads configuration data from external memory. The BST18V04 is designed to be directly compatible with the main string mode of the FPGA.

When starting or reconfiguring, as long as the three mode selection pins of the FPGA are all low (M0=0, M1=0, M2=0), the FPGA enters the master serial mode. Data is read serially from a data line of the BST18V04. The BST18V04 and the FPGA are synchronized by the rising edge of the clock signal CCLK generated during the configuration process.

The master serial mode provides a simple configuration interface. There is only one serial data line and two control lines to configure the FPGA. The internal address and bit counter counts at each valid CCLK rising edge, and the data is read serially from the BST18V04 under the control of the counter.

If the user-programmable bidirectional Din pin on the FPGA is used only for configuration (it must be kept at a fixed level during normal operation), the FPGA automatically solves this problem through the default pull-up resistor inside the chip.

8.3. Cascade Configuration Summary

When multiple FPGAs are configured in serial or parallel, or a single FPGA requires a large amount of configuration data, cascaded PROMs can provide more storage space. Multiple BST18V04s can be cascaded by using the CEO of the previous PROM to drive the CE pin of the next PROM. The clock and data pins of all cascaded BST18V04s will be connected together. After the last data of the first PROM is output, the PROM will set the CEO pin to a low level at the next clock and drive the data pin to a high impedance state, and then the CE pin of the second PROM will become a low level, thereby configuring the data output.

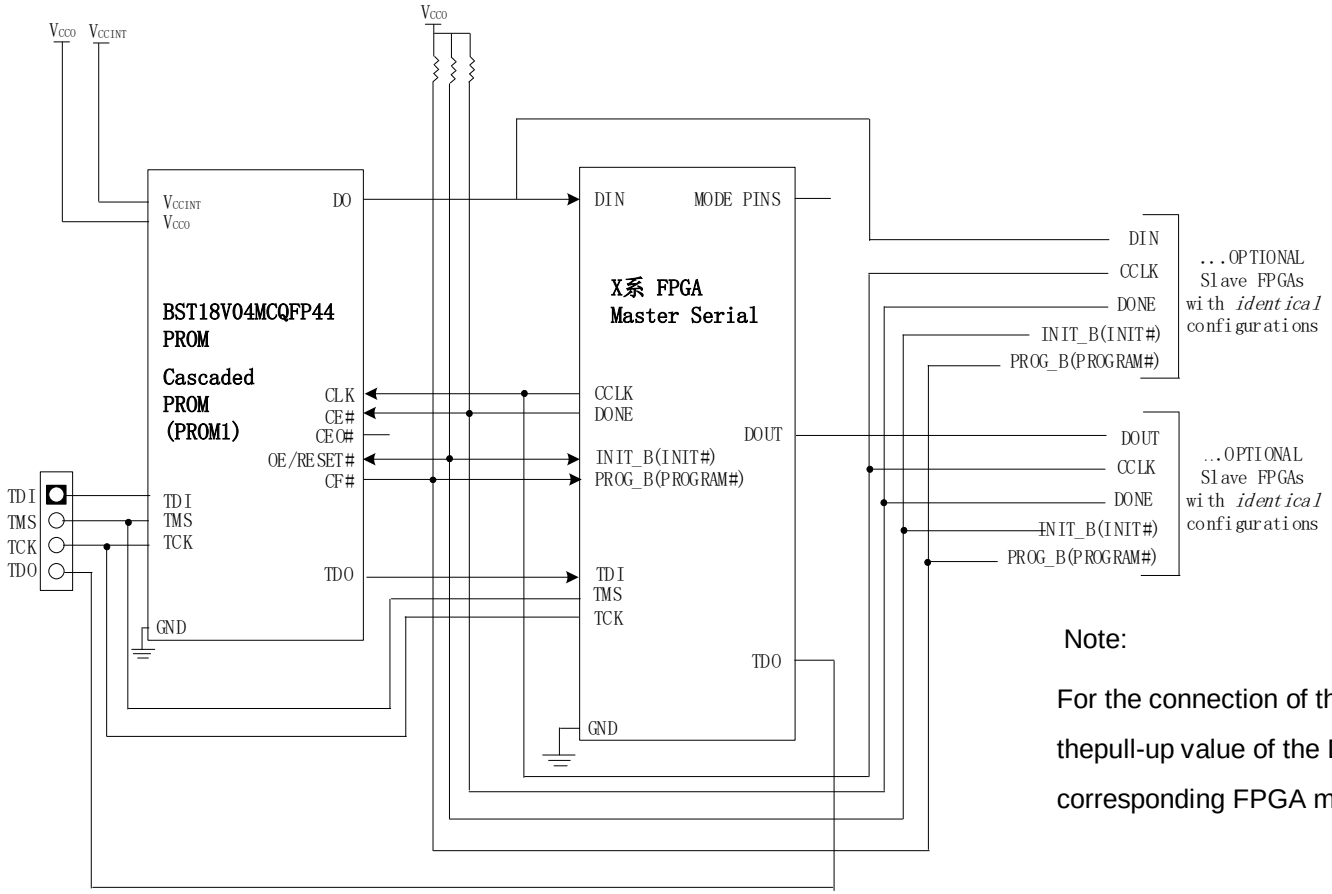
After configuration is completed, OE/RESET going low or CE going high will reset the addresses of all cascaded PROMs.

8.4. Initialize FPGA configuration

BST18V04 includes a CF pin that can be controlled by JTAG instructions. BST18V04 can send a low pulse of about 500ns to FPGF through the CF terminal to reconfigure the FPGA, reset the FPGA and restart the configuration of the FPGA. The CF pin of BST18V04 must be connected to the PROGRAM pin of the FPGA to use this function.

/8.5. Select Configuration Mode

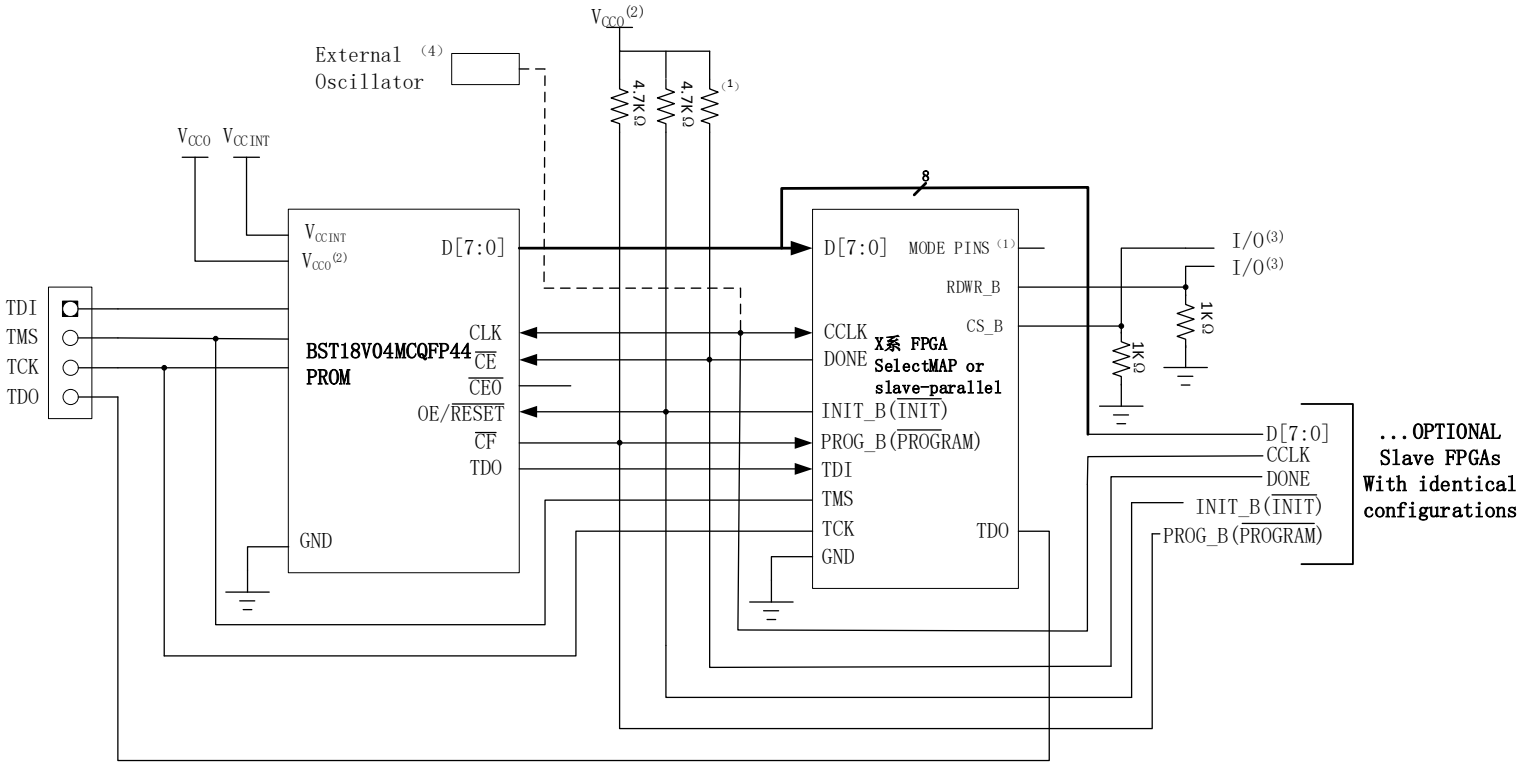
BST18V04 can choose serial and parallel configuration modes. Changing the configuration mode is achieved by changing the control register in the chip. When in use, the configuration mode (serial or parallel) can be changed through Xilinx iMPACT software. The FPGA defaults to serial mode.



Picture 5. Main String Mode

Note:

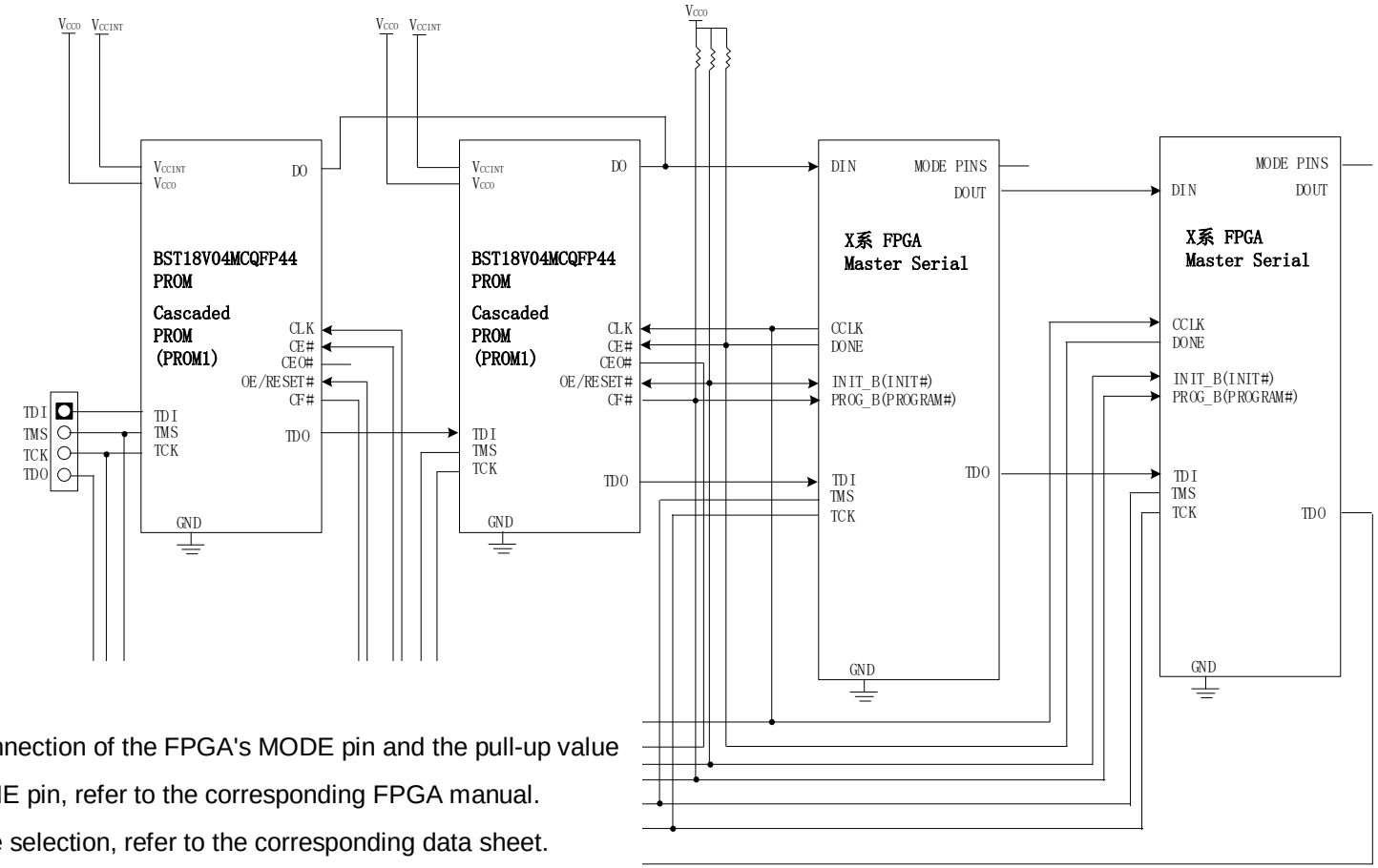
For the connection of the FPGA's MODE pin and thepull-up value of the DONE pin, refer to the corresponding FPGA manual.



Picture 6. Master/Slave SelectMAP or Parallel Mode

Note:

- For the connection of the FPGA's MODE pin and the pull-up value of the DONE pin, refer to the corresponding FPGA manual.
- For voltage selection, refer to the corresponding data sheet.
- The CS_B (or CS) and RDWR_B (or WRITE) pins must be driven low or pulled down.
- For Virtex/Virtex-E SelectMAP configuration mode, Virtex-II/Virtex-II Pro Slave SelectMAP configuration mode, and Spartan-II/Spartan-IIE Slave Parallel configuration mode, an external crystal is required.

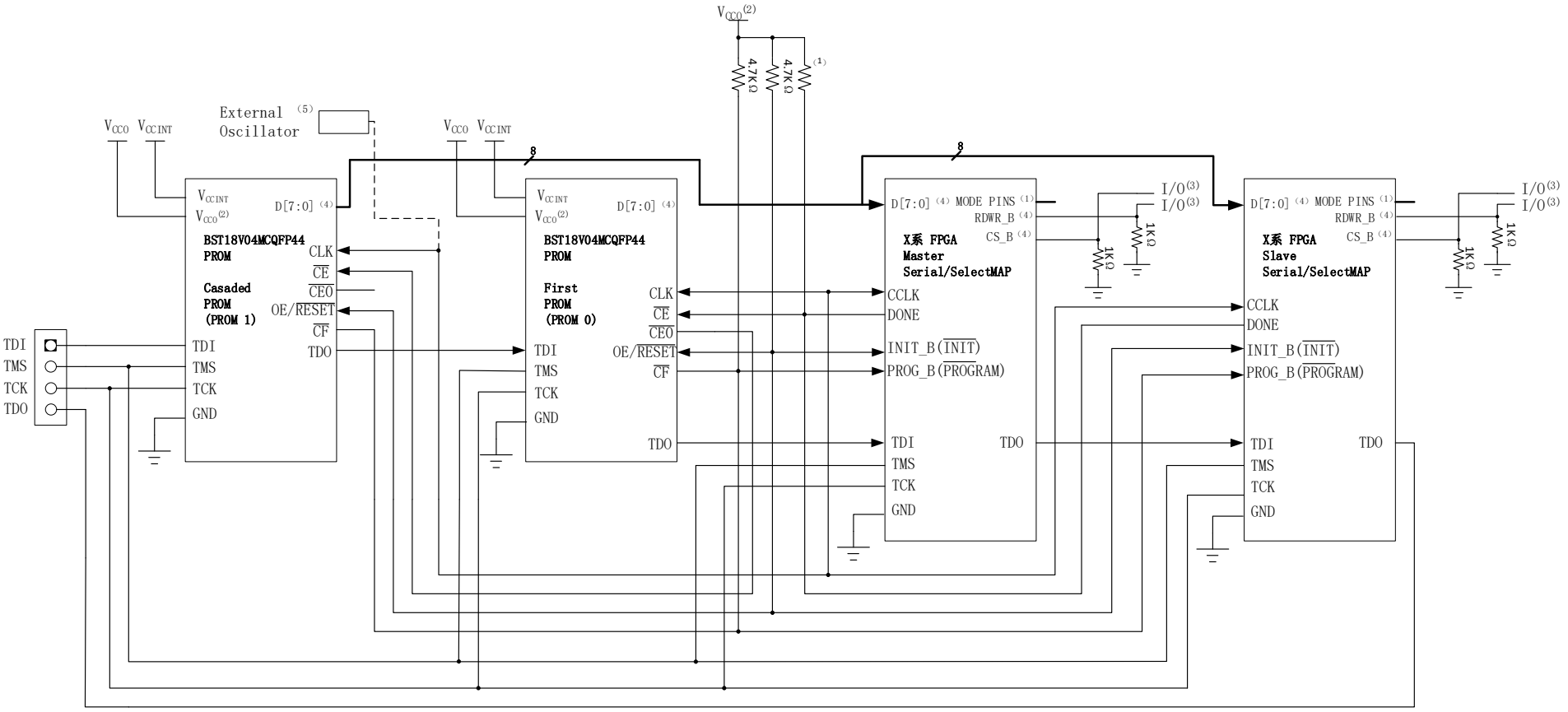


Note:

For the connection of the FPGA's MODE pin and the pull-up value of the DONE pin, refer to the corresponding FPGA manual.

For voltage selection, refer to the corresponding data sheet.

Picture.7. Master/Slave Serial Mode to Configure Multiple Devices



Picture 8. Configure multiple devices using Master/Slave Serial, Master/Slave SelectMAP, or Master/Slave Parallel configurations

Note:

- For the connection of the FPGA's MODE pin and the pull-up value of the DONE pin, refer to the corresponding FPGA manual.
- For voltage selection, refer to the corresponding data sheet.
- For SelectMAP mode, CS_B (or CS) and RDWR_B (or WRITE) must be driven low or pulled low.
- The serial mode does not require the D[7:1], CS_B, and RDWR_B pins to be connected.
- When CLK is not provided by the FPGA in master mode, an external crystal oscillator is required.

8.6. How to use 8Mb mode

The 8Mb mode requires sending instructions through the JTAG terminal to set the chip to 8Mb storage capacity.

At the same time, it is necessary to combine the self-developed software of Chengdu Huawei and the use of ISE to complete the operation of Flash. For detailed operations, please refer to "mcs2svf software instructions" and "CSMT JTAG programmer manual.doc".

8.7. Configuring storage requirements

Table 3. FPGA configuration storage requirements

FPGA Devices	Configuration bits	4Mb Mode	8Mb mode
BST2V1000	3,752,736	1	1
BST2V3000	9,594,656	3	2
BST2V6000	19,759,904	5	3

Table 4. BST18V04MCQFP44 storage capacity

Devices	Configuration bits (4Mb)	Configuration bits (8Mb)
BST18V04	4,194,304	8,388,608

IX. Operating procedures and precautions

The input and output operation timing of the chip is defined in accordance with the chip's instruction manual. This section mainly focuses on the precautions during welding and debugging.

Anti-static packaging is used during transportation, but if you are not careful during the

entire process from before and after welding to the completion of debugging and assembly of the board into the chassis, it will cause classic damage and reduce the reliability of the integrated circuit. Therefore, you need to pay attention to the following points:

- When opening a package, it must be done in an anti-static place, especially in cold and dry seasons. Operators should consciously release static electricity from their bodies. I believe that many people have been hit by door handles in dry and cold weather. At this time, the static electricity can reach tens of thousands of volts, which is unbearable for general integrated circuits. How to release static electricity? If conditions permit, you can use particle wind, wear an anti-static wristband, etc. If conditions do not permit, you can release it by touching a grounded computer case.
- Welders must operate on an anti-static table. Even if they wear an anti-static wristband, they should not touch the pins when handling the chip. They are not allowed to accidentally touch clothing, ordinary plastics and other items that are prone to static electricity. Chips must be packaged in a special anti-static bag. Electric soldering irons must be anti-static.
- During the test and adjustment process, the debugging personnel should pay attention to prevent high-static items such as clothing from coming into contact with the printed circuit boards and components, and try to hold the printed circuit boards by the edges.
- Be very careful when the test equipment and chip power supply are not in the same ground, as the accumulated potential difference may cause discharge.

X. Product Ordering Information

Product model	Package	Lead Material	Encapsulation type	Dimensions (mm)	weight	Detailed Specification No.	Quality grade
BST18V04MCQFP44	CQFP44	Gold plating	Airtight packaging	13*13*2.15	≤0.85g	Q/BST 20435-2019	GJB597B-2012 Class B
BST18V04ETQFP44	TQFP44	Tinning	Non-hermetic packaging	12*12*1.6	≤0.4g	Q/BST 50158-2021	Chengdu Huawei Enterprise Standard Military Temperature Grade

- Precautions for installation and use hardware

  This software currently only supports parallel download cables. When using, connect one end of the parallel download cable toPCThe parallel port of the machine (usuallyLPT1port), one end is connected to the corresponding chip JTAG. The programming pins are connected. For specific connection methods, please refer to the cable instructions.

  - Installation Environment

    Operating system:Windows 2000and above.

    You must have system administrator privileges to install and use it.

    Run CSMT_JTAGProgrammer_setup.exe, follow the prompts to select the appropriate path to complete the installation.

  - Supported Devices

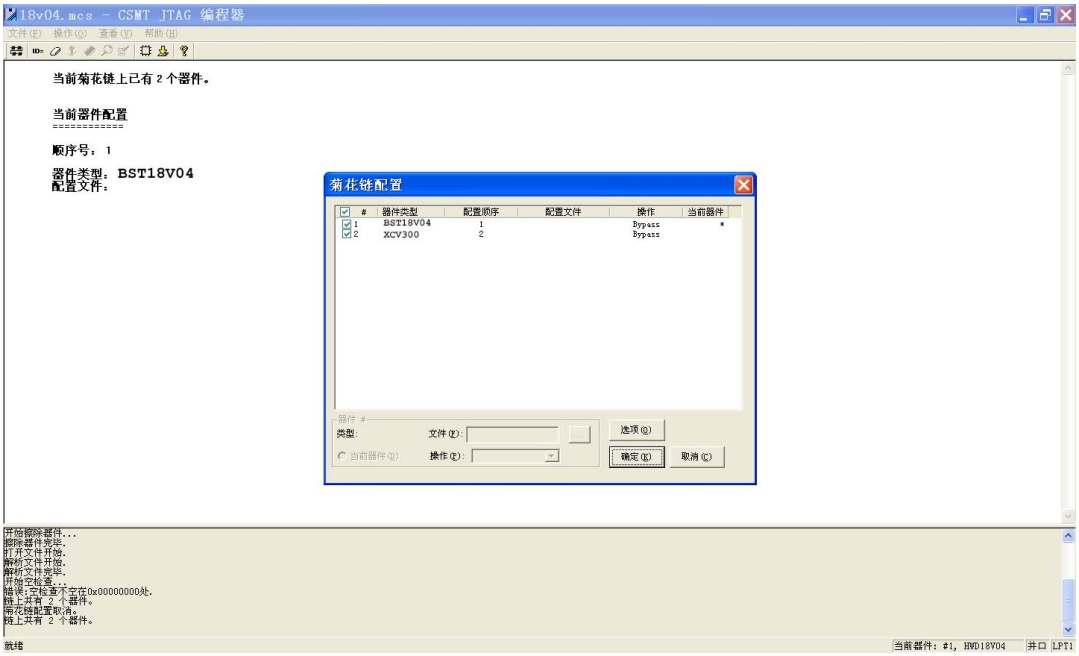
    BST1400 series CPLD——Please use the CPLD version programming software

BST18V04 E2PROM——Please use BST18V04 cascade special version

Support Xilinx Virtex series FPGA cascade display (can identify this series of FPGA and read Device ID and User ID, but does not support direct programming)

- Startup

  The interface after starting the software is as shown below:



Appendix. Figure 1. Software Startup Screen

- User Guide

  Start up

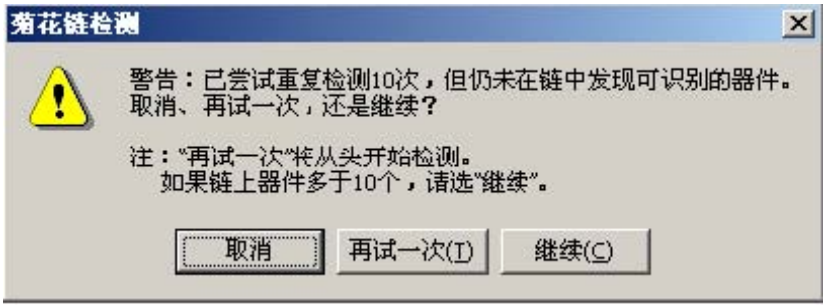
  After startup, the program will automatically check the daisy chain. During the

daisy chain check, the following situations will pop up:“Daisy chain detection warning message box”(As shown in the figure2shown):

Device not powered ;

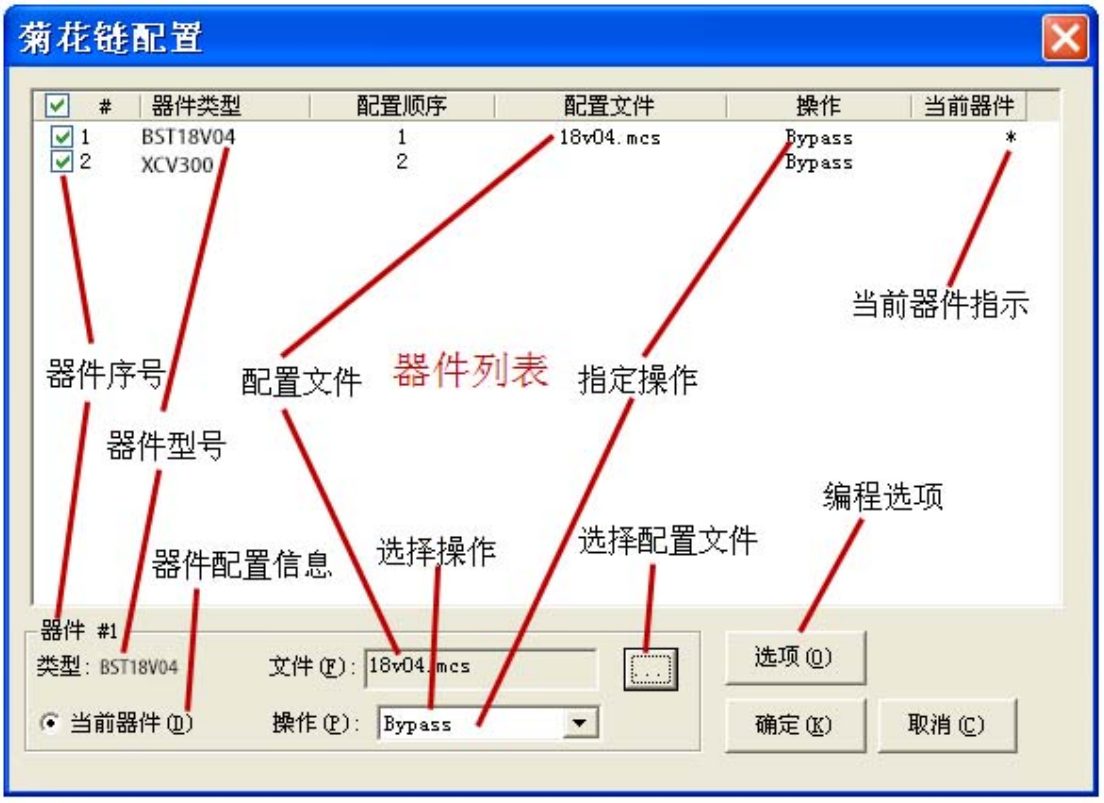
No identifiable device on the chain ;

The number of devices exceeds the default value of the program (10indivual).



Appendix Figure 2. Daisy chain check warning message

If the daisy chain check passes, then the “Daisy Chain Configuration Dialog Box” Configure the daisy chain. As shown in the following figure:



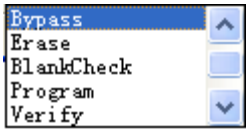
Appendix. Figure 3. Daisy Chain Configuration Dialog Box

- Erase, Program

  This software supports MCS Configuration file format.

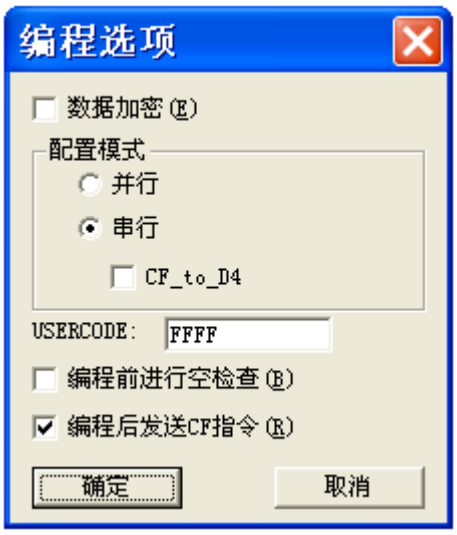
  Configure the Flash device, click the Select File button  When the file selection box pops up, the user specifies MCS document.

  Select one of the following options :Bypass, Erase, Blank check, Program, Verify, as shown in the figure4(Note: The current software can only execute Bypass, Erase, Program)



Appendix. Figure 4. Operation drop-down menu

Options: Click “Options” The button will pop up “Programming Options Dialog Box” Figure 5 shows options for setting the encryption bit, serial-to-parallel conversion bit, etc.



Appendix. Figure 5. BST18V04 Programming Options Dialog Box

Erase: Select the menu command [Operation → Erase] or click button to perform the erase operation.

Programming: Select the menu command: [Operation → Programming] or click the button to perform programming operations. “Programming Options Dialog Box”(As shown in Figure 5). When programming is completed, the dialog box shown in Figure 6 will pop up.

Appendix. Figure 6. BST18V04 programming completed

- Toolbar Reference:

 Initialize the Daisy Chain

 Read the manufacturer of the current deviceID

 Block Erase

 programming

 Configuring a Daisy Chain

12.2. MCS2SVF software instructions

mcs2svf version software in BST18VDeveloped based on the 8M programming version of 04, an MCS to SVF column is added to the operation options in the menu bar.

- MCS to SVF can be used without connecting download cables and devices.
- Cascade adjustment: Find the cascade information generated after modifying the configuration file cascade. cfg in the installation directory.
- Supports generating SVF from a single 4M MCS data (load file 1 separately and click Generate), or generating an 8M SVF data file from two 4M MCSs (load both file 1 and file 2 and click Generate).
- Can generate SVF files containing serial or parallel programming mode.