

BST16PFPGA supporting memory

Product Brochure

Ver 3.00

Revision History

Edition	Change Description	Change order number	Change Person	Change Date	Remark
V1.00	Initial release	NA	Que Xiaoqian	2012/3/1	
V2.00	Add power supply sequence requirements	NA	Que Xiaoqian	2019/1/29	
V3.0	Add Notes	NA	Que Xiaoqian	2020/11/18	

I. Product Overview

The BST16P has a storage capacity of 16Mbits and provides an easy-to-use, cost-effective and reprogrammable method for Xilinx FPGA configuration information. The BST16P supports master-serial, slave-serial, master-parallel and slave-parallel FPGA configuration modes.

Features are as follows:

- In-circuit programmable PROMs can configure Xilinx FPGAs
- The latest low-power BSTOS NOR flash structure
- Supports 20,000 program/erase cycles
- Fully supports industrial -55 to +125 °C variations
- Support IEEE 1149.1/1532 protocols

- JTAG commands can be used to initialize FPGA configuration
- Supports cascading storage of longer or multiple bitstreams
- Dedicated I/O voltage for JTAG boundary scan (VCCJ)
- The I/O power supply voltage is 3.3V and the core voltage is 1.8V
- 1.8V core voltage
- Design versioning technology allows storing and accessing multiple configuration versions
- Hardware data decompression supports Xilinx's latest compression technology

II. Application

BST16P supports Xilinx FPGA series.

III. Pin Arrangement

Table 1. BST16P pin description

Pin Name	Boundary Scan order	Boundary Scan Function	Pin Description	48-pin FBGA
D0	28	Data Output	D0 is the data output port for FPGA serial configuration. D0-D7 are the data output ports for FPGA parallel mode. DO is high impedance when ISPEN (not clamped). D1-D7 are high impedance when ISPEN (not clamped) and when in serial mode. D1-D7 can be unconnected when the PROM is used in serial mode.	H6
	27	Output Enable		
D1	26	Data Output		H5
	25	Output Enable		
D2	22	Data Output		E5
	23	Output Enable		
D3	22	Data Output		D5
	21	Output Enable		

Pin Name	Boundary Scan order	Boundary Scan Function	Pin Description	48-pin FBGA
D4	20	Data Output		C5
	19	Output Enable		
D5	18	Data Output		B5
	17	Output Enable		
D6	16	Data Output		A5
	15	Output Enable		
D7	14	Data Output		A6
	13	Output Enable		
CLK	1	Data Entry	Configuration clock input. An internal programmable control bit selects the internal crystal or CLK input as the configuration clock. If CLK is valid, the internal counter increases on each rising edge of the CLK input. $\overline{OE}/\overline{RESET}$ For low, $\overline{CE}$ is high, BUSY is low (parallel mode), $\overline{CE}$ When not driven, it is pulled down to logic 0 by the pull-down resistor.	B3
$\overline{CE}$	4	Data Entry	When low, holds the counter reset and the DATA and CLKOUT outputs in a high-impedance state.	A3
	3	Data Output		
	2	Output Enable		
$\overline{CE}$	0	Data Entry	Chip Enable Input. $\overline{CF}$ When high, the device enters sleep mode, the counter is reset and DATA and CLKOUT are placed in high impedance state.	B4
$\overline{PROGRAM}$	11	Data Entry	As output, $\overline{CF}$ Run the JTAG CONFIG instruction to initialize the FPGA configuration without powering down the FPGA. $\overline{CF}$ At the rising edge of , the current design	D1
	10	Data Output		
	9	Output Enable		

Pin Name	Boundary Scan order	Boundary Scan Function	Pin Description	48-pin FBGA
			version is sampled and the internal counter is reset to the initial address of the selected version. $\overline{\text{PROGRAM}}$ If not used, $\overline{\text{CF}}$ Must be pulled up to VCCO by an external 4.7k Ω resistor.	
$\overline{\text{CEO}}$	6	Data Output	In the cascade, $\overline{\text{CF}}$ Connected to the next PROM $\overline{\text{CF}}$ port. $\overline{\text{CF}}$ For low and $\text{OE}/\overline{\text{RESET}}$ It is low when it is high and when the internal counter reaches its maximum value or when the PROM does not respond to any version selection. $\overline{\text{WRITE}}$ exist $\overline{\text{CEO}}$ Low or $\overline{\text{CE}}$ becomes high when is high.	D2
	5	Output Enable		
$\text{OE}/\overline{\text{RESET}}$	31	Data Entry	When it is low, the design version selection is controlled by the external port, and when it is high, the design version is controlled by the internal programmable control. $\overline{\text{CE}}$ Pulled up to logic 1 by an internal resistor.	H4
REV_SEL0	30	Data Entry	Version selection input. $\overline{\text{CE}}$ When low, the version is selected by the version select port and overrides the internal configuration selection bits. REV_SEL [1:0] is pulled up to logic 1 by internal resistors when not driven.	G3
REV_SEL1	29	Data Entry		G4
BUSY	12	Data Entry	BUSY is valid only when configured for parallel mode. When BUSY is high, the internal address counter stops counting and the current data is held at the data port. Once CLK generates a rising edge and BUSY goes low, the data of the next address is driven to the data port. BUSY is	C1

Pin Name	Boundary Scan order	Boundary Scan Function	Pin Description	48-pin FBGA
			invalid when serial or decompression is valid. BUSY is pulled down to logic 0 by an internal resistor when there is no driver.	
CLKOUT	8	Input and Output	The internal bit controls CLKOUT to select the internal crystal or external CLK input. If the data is valid, the internal address counter increases on each rising edge of the clock. $\overline{CE}$ For low, $OE/\overline{RESET}$ is high. Output data is valid on every rising edge of $\overline{CLKOUT.CF}$ High or $rPROGRAM$ If CLKOUT is low, CLKOUT is invalid. If decompression is valid, CLKOUT is set high when decompressed data is not ready. When CLKOUT is invalid, the CLKOUT port is set to high impedance. If CLKOUT is used, it must be pulled up externally with a 4.7kΩ resistor.	C2
	7	Output Enable		
TMS	-	Mode Selection	JTAG mode select input. TMS is transmitted to the internal TAP controller on each rising edge of TCK. TMS is pulled up to VCCJ by an internal resistor for logic 1.	E2
TMS	-	clock	JTAG clock input. It controls the TAP controller and all JTAG testing and programming.	H3
TDI	-	Data Entry	JTAG serial data input. This port serially inputs data to JTAG instructions or register data. When not driven, it is pulled up to VCCJ by an internal resistor for logic 1.	G1
TDO	-	Data Output	JTAG serial data output. The port serially shifts out all JTAG instructions and data register values. When not driven, it is pulled up to	E6

Pin Name	Boundary Scan order	Boundary Scan Function	Pin Description	48-pin FBGA
			VCCJ by an internal resistor to logic 1.	
VCCINT	-	-	1.8V power supply, positive 1.8V internal logic power supply	B1, E1G6
VCCO	-	-	3.3V power supply. Provides positive 3.3V power supply for output voltage drive and input BUFF	B2, C6, D6, G5
VxJ	-	-	3.3V JTAG I/O power supply, provides positive 3.3V power for TDO output voltage driver and TCK, TMS and TDI input BUFF.	H2
GND	-	-	land	A1, A2, B6, F1, F5, F6, H1
DNC	-	-	No connection	A4, C3, C4, D3, D4, E3, E4, F2, F3, F4, G2

IV. Block Diagram

The block diagram of the BST16P working platform is shown in Figure 1 below:

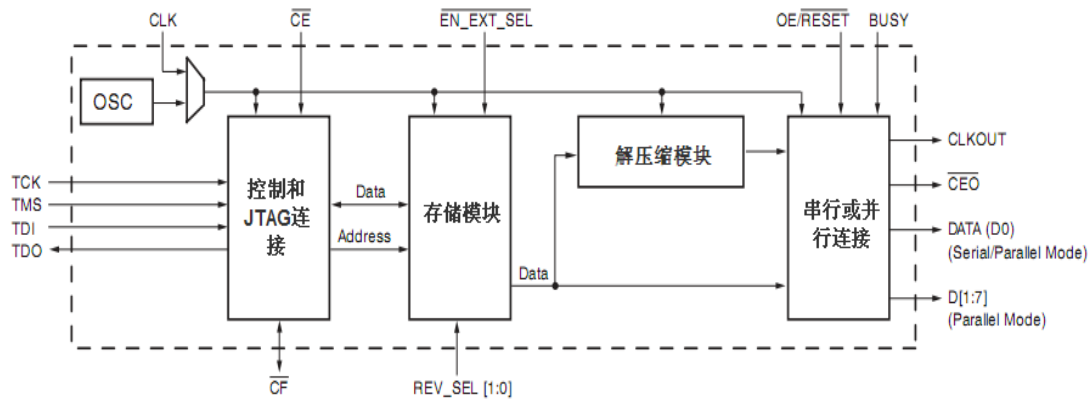


Figure 1. BST16P structure diagram

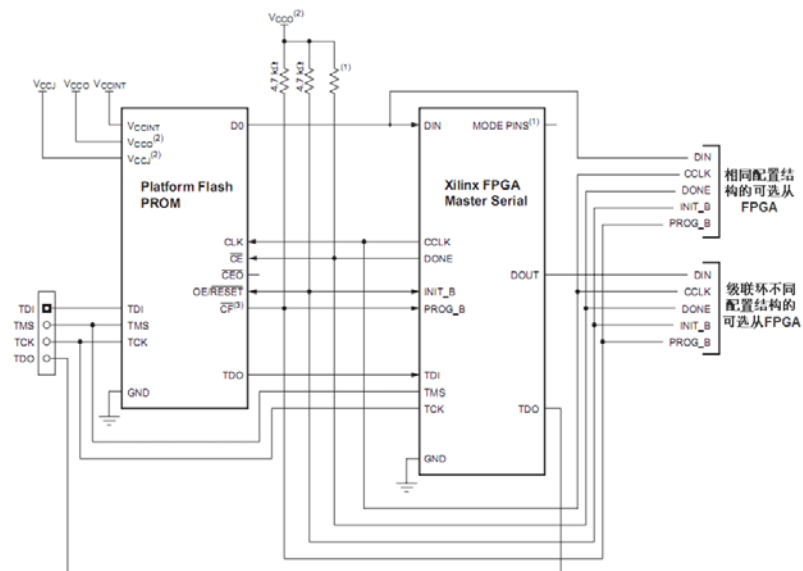


Figure 2. Main string mode configuration

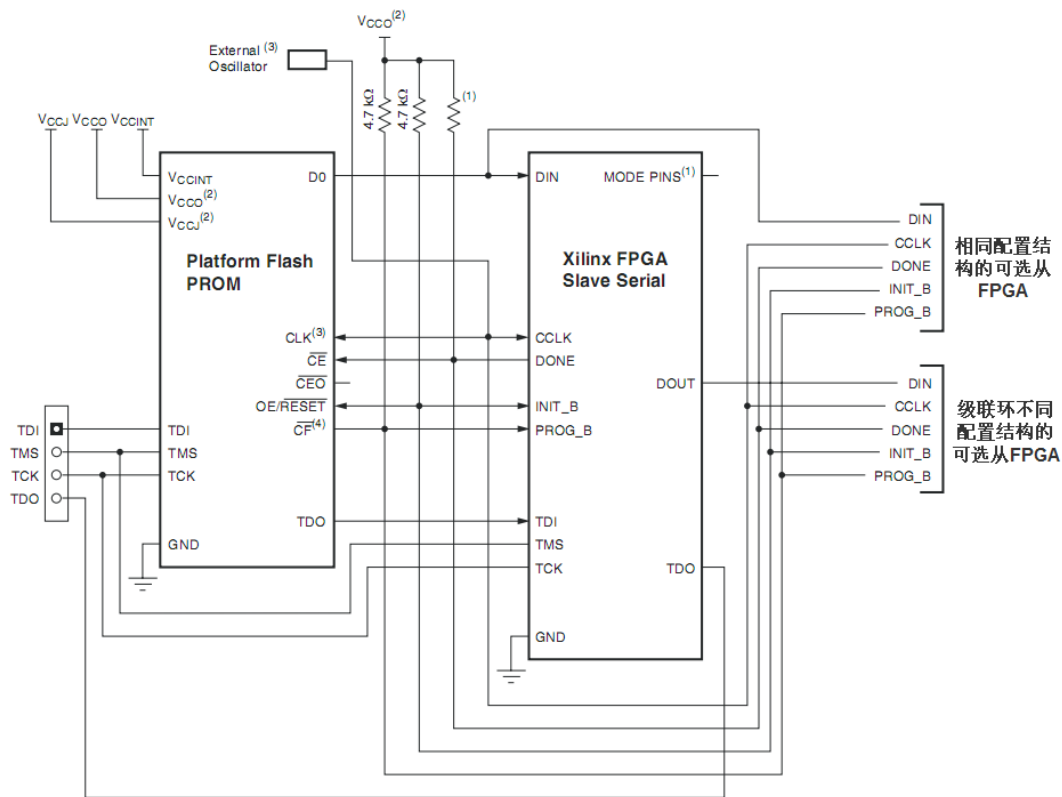


Figure 3. Slave mode configuration

V. Maximum Ratings Parameters

Table 2. Maximum ratings

Core supply voltage (V_{CCINT})	-0.5V~2.7V
I/O supply voltage (V_{CCO})	-0.5V~4.0V
JTAT I/O supply voltage (V_{CCJ})	-0.5V~4.0V
DC input voltage to ground (V_{IN})	-0.5V~3.6V
Three-state output voltage to ground (V_{TS})	-0.5V~3.6V
Storage temperature (T_{STG})	-65°C~150°C

Lead soldering temperature (TSOL)	260°C
Junction temperature (TJ)	175°C

VI. Recommended operating conditions

Core power supply voltage (VCCINT) 1.8V

I/O supply voltage (VCCO) 3.3V

JTAG supply voltage (VCCJ) 3.3V

Input low level voltage (VIL) 0.8V

Input high level voltage (VIH) 2.0V

Working environment temperature (TA) -55°C~125°C

VII. Electrical properties

Unless otherwise specified, the electrical characteristics shall be as specified in Table 3 and shall apply over the full operating temperature range.

Table 3. Electrical characteristics

Characteristic	Symbol	Condition Unless otherwise specified VCCINT=1.8V VCCO=3.3V -55°C≤TA≤125°C	Group A Grouping	Limit value		unit
				Minimum	Maximum	
Output high level voltage	VOH	VCCO=3.3V When IOH = -4 mA	A1	2.4	-	V
Output low level voltage	VOL	VCCO=3.3V IOL = 4 mA	A2	-	0.4	V
Input high level voltage	VIH	VCCO=3.3V	A3	2.0	3.6	V
Input low level voltage	VIL	VCCO=3.3V		0	0.4	V

Characteristic	Sym- bol	Condition Unless other- wise specified $V_{CCINT}=1.8V$ $V_{CCO}=3.3V$ $-55^{\circ}C\leq T_A\leq 125^{\circ}C$	Group A Group- ing	Limit value		unit
				Mini- mum	Maxi- mum	
Nuclear power supply operating current	I_{CCINT}	f=33 MHz		-	20	mA
IO power supply operating cur- rent a	I_{CCO}	Serial f = 33 MHz		-	20	mA
		Parallel f=33 MHz		-	50	mA
Core power supply current b in standby	I_{CCINTS}			-	2	mA
IO power supply current b in standby	I_{CCOS}			-	2	mA
JTAG download terminal TMS, TDI and TDO pull-up current	I_{ILJ}	$V_{CCJ}= \text{max}, V_{IN} = \text{GND}$		-	100	uA
Input leakage current	I_{IL}	$V_{CCINT}= \text{max}, V_{CCO} = \text{max}$ $V_{IN} = \text{GND or } V_{CCO}$		-10	10	uA
EN_EXT_SEL_ \ REV_SEL0 REV_SEL1 pin internal pull-up current	I_{ILP}	$V_{CCINT}= \text{max}, V_{CCO} = \text{max}$ $V_{IN}= \text{GND or } V_{CCO}$		-	100	uA
BUSY and CLK pin internal pull- down current	I_{IHP}	$V_{CCINT}= \text{max}, V_{CCO} = \text{max}$ $V_{IN}= \text{GND or } V_{CCO}$		-100	-	uA
PROM is in slave mode:						
Guaranteed version instantiation CF_hold time	t_{HCF}		A9 A10 A11	300	-	ns
CE_ to data delay time c	t_{CE}			—	25	ns
OE/RESET_ to data delay time d	t_{OE}			—	25	ns
Guarantee the holding time c of CE_ to reset the counter	t_{HCE}			2000	—	ns
OE/RESET_ hold time d to en- sure counter reset	t_{HOE}			2000	—	ns
EN_EXT_SEL_ setup time rela- tive to CF_ \ CE_ or OE/RESET_	t_{SXT}			300	—	ns

Characteristic	Sym- bol	Condition Unless other- wise specified $V_{CCINT}=1.8V$ $V_{CCO}=3.3V$ $-55^{\circ}C\leq TA\leq 125^{\circ}C$	Group A Group- ing	Limit value		unit
				Mini- mum	Maxi- mum	
EN_EXT_SEL_ hold time rela- tive to CF_ \ CE_ or OE/RESET_	t _{HXT}			300	—	ns
REV_SEL setup time relative to CF_ \ CE_ \ OE/RESET_	t _{SRV}			300	—	ns
REV_SEL hold time relative to CF_ \ CE_ or OE/RESET_	t _{HRV}			300	—	ns
CLK to data delay	t _{CAC}			—	25	ns
In serial mode, the minimum clock cycle f	t _{CYC}			25	—	ns
In parallel mode, the minimum clock cycle f				40	—	ns
CLK minimum low level time g	t _{LC}			12	—	ns
CLK minimum high level time g	t _{HC}			12	—	ns
CE_ setup time relative to CLK (to ensure correct counting) g	t _{SCE}			50	—	ns
PROM main mode:						
Guaranteed version instantiation CF_ hold time	t _{HCF}		A9 A10 A11	300	-	ns
CE_ to data delay time c	t _{CE}			—	25	ns
OE/RESET_ to data delay time d	t _{OE}			—	25	ns
Guarantee the holding time c of CE_ to reset the counter	t _{HCE}			2000	—	ns
OE/RESET_ hold time d to en- sure counter reset	t _{HOE}			2000	—	ns
EN_EXT_SEL_ setup time rela- tive to CF_ \ CE_ or OE/RESET_	t _{SXT}			300	—	ns
EN_EXT_SEL_ hold time rela- tive to CF_ \ CE_ or OE/RESET_	t _{HXT}			300	—	ns
REV_SEL setup time relative to CF_ \ CE_ \ OE/RESET_	t _{SRV}			300	—	ns

Characteristic	Sym- bol	Condition Unless other- wise specified V _{CCINT} =1.8V V _{CCO} =3.3V -55°C≤TA≤125°C	Group A Group- ing	Limit value		unit
				Mini- mum	Maxi- mum	
REV_SEL hold time relative to CF_ \ CE_ or OE/RESET_	t _{HRV}			300	—	ns
CE_ to CLKOUT delay h	t _{CECC}			0	2CLK cycles	
Delay from OE/RESET_ to CLKOUT h	t _{OECC}			0	2CLK cycles	
CLKOUT to Data Delay	t _{CCDD}			—	30	ns
When decompressing, the data setup time relative to CLKOUT is i	t _{DDC}			5	-	ns
When decompressing, the data is kept at CLKOUT for a certain period of time.	t _{COH}			3	—	ns
CLK input to CLKOUT output delay	t _{CLKO}			—	35	ns
In serial mode, the minimum duty cycle j	t _{CYCO}			30	—	ns
In parallel mode, the minimum duty cycle j				40	—	ns
CLK minimum low level time	t _{LC}			12	—	ns
CLK minimum high level time	t _{HC}			12	—	ns
Note: When powered on, the device requires VCCINT to rise monotonically and smoothly to the operating voltage within 0.2ms to 35ms.						

Characteristic	Sym- bol	Condition Unless other- wise specified V _{CCINT} =1.8V V _{CCO} =3.3V -55°C≤TA≤125°C	Group A Group- ing	Limit value		unit
				Mini- mum	Maxi- mum	
• The supplementary current specification of the driver output is based on no-load conditions; • CE_high, OE/RESET_low, TDI\TMS\TCK static; • If tHCE high level <2us, tCE = 2us; • If tHOE low level <2us, tOE = 2us; • Guaranteed by design, not tested; • This is the minimum tCYC. The actual tCYC = tCAC + FPGA data setup time. • All AC parameters are measured with VIL = 0.0V and VIH = 3.0V; • This parameter depends on the configuration clock and becomes larger when decompression is enabled; • When decompression is enabled, the CLKOUT signal is the control clock output. When decompressed data arrives, CLKOUT is locked to 1/2 of the source clock frequency. (1/2 of the selected internal clock or external clock frequency input by CLK). When decompressed data does not arrive, the CLKOUT pin is pulled high. If the CLKOUT signal is used, it must be pulled up to VCCO with a 4.7KΩ resistor externally. • This is the minimum TCYCO, the actual tCYCO = tCCDD + FPGA data setup time.						

VIII. Typical operating characteristics

When the FPGA is in master serial mode, the FPGA will generate a configuration clock that drives the PROM. $\overline{CE}$ For high, $\overline{OE}/\overline{RESET}$ The PROM data port is connected to the FPGA data port within a certain access time after the OE is valid. The new data will be effectively output after each rising edge of the clock. At the same time, the FPGA will generate an output pulse to complete the configuration.

When the FPGA is in slave mode, both the PROM and the FPGA are controlled by external clocks, and the BST16P PROM can be used to drive the FPGA's configuration clock. The BST16P platform's PROM can support both master-parallel and slave-parallel FPGA configuration modes. When the FPGA is in master-parallel mode, the FPGA generates a configuration clock to drive the PROM. When the FPGA is in slave-parallel mode, the

external crystal oscillator generates a configuration clock to drive the PROM and FPGA, and the BST16P PROM can also be used to drive the FPGA's configuration clock. $\overline{CE}$ For low, $\overline{CE}$ For high, $OE/\overline{RESET}$ After the OE is valid, the data on the PROM data port is valid, and the FPGA will sample the data at each CCLK rising edge. An independently running crystal oscillator can be used in slave parallel mode.

The BST16P version of the Flash PROM platform provides additional new features. Hardware data decompression can support compressed PROM files, and the design version technology allows multiple design versions to be stored in a single PROM or cascaded multiple PROMs. To implement the design version, the design version function can be activated by selecting an external port or an internal control bit.

The Flash PROM platform is compatible with all existing FPGA device families.

IX. Test Circuit

The test circuit of BST16P is as follows:

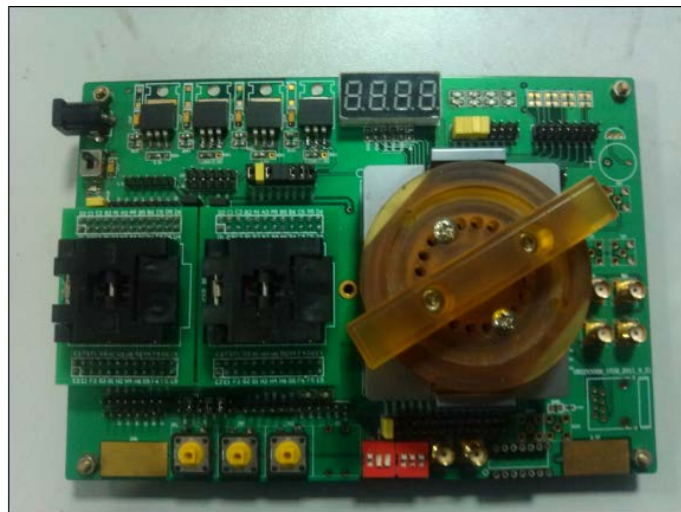


Figure 4. BST16P functional test board

XX. Switching Characteristics

Power-on sequence requirements: VCCINT is powered on first, and VCCO is powered on later.

- Power-On Reset

When powered on, the device requires the voltage VCCINT to provide a monotonic and stable rising control voltage within the rising time. If the power supply cannot meet the requirements, the device may not be able to perform the power-on reset function. During the timing power-on period, $\overline{CF}$ Once the power supplies reach their respective POR (PRESET) turn-on limits, the delay (minimum $\overline{CF}$) release $\overline{CF}$, to allow more margin for the power supply to stabilize before configuration. $\overline{CF}$ The port is connected to an external pull-up resistor and the INIT port of the FPGA. When the power supply rises slowly, an additional voltage monitoring circuit is fixed $\overline{OE}/\overline{RESET}$ is low, delaying configuration until the system power reaches the minimum operating voltage. $\overline{OE}/\overline{RESET}$ When released, the FPGA initialization port is pulled high and allows the FPGA timing configuration. $\overline{CE}$), the PROM is reset, $\overline{CE}$ It is pulled low again until the POR limit voltage value. $\overline{CE}$ The polarity is not editable. The turn-on conditions are shown in the figure.

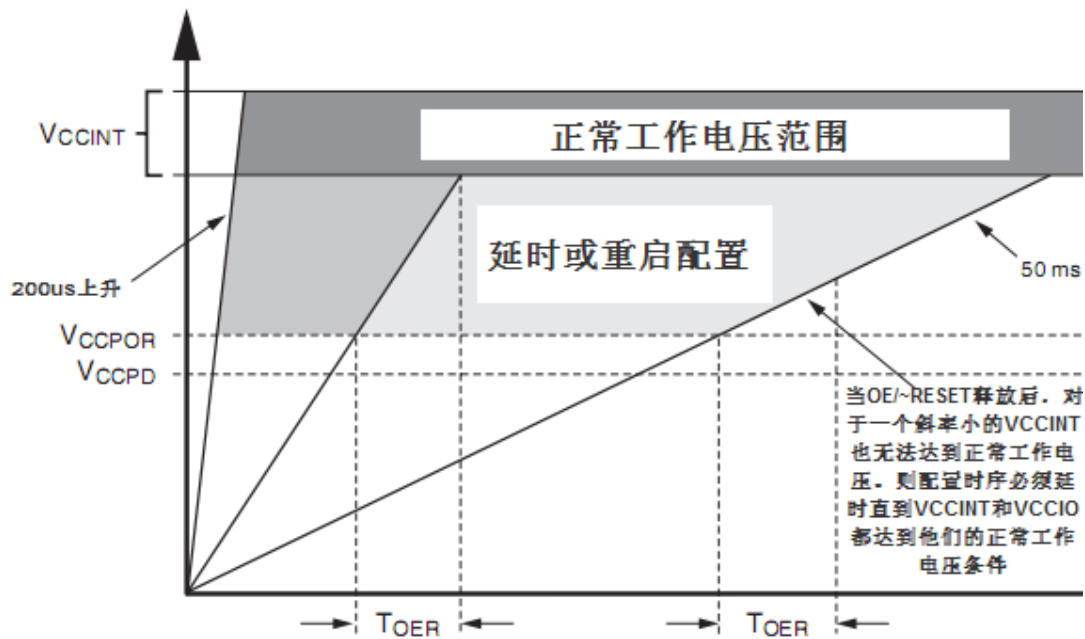


Figure 5. PROM power-on requirements

The voltage conditions for powering on and off are shown in the following table:

Table 4 Power-on and power-off requirements

Signal	Describe	BST16P		Unit
		Min	Max	
TVCC	The rise time of VCCINT from 0 to normal voltage	0.2	50	ms
VCCPOR	VCCINT POR start-up limit voltage	0.5	-	V
TOER	After POROE/ $\overline{\text{RESET}}$ Delay time	0.5	30	ms
VCCPD	VCCINT shutdown limit voltage	-	0.5	V

Note:

There is no restriction on the power supply sequence of VCCINT, VCCO, and VCCJ.

When powered on, the device requires the VCCINT power supply to automatically rise to the normal operating voltage range within the TVCC time.

If in $\overline{\text{CF}}$ Before release, if VCCINT and VCCO have not reached the normal

operating voltage range, the configuration data from the PROM is not available.

The configuration sequence must be delayed until both VCCINT and VCCO reach their normal operating range.

- Sleep Mode

When $\overline{CE}$ When high, the PROM will enter a low power sleep mode. In sleep mode, the address counter is reset. $OE/\overline{RESET}$ is driven high, the other outputs are placed in a high impedance state and ignored. $\overline{CF}$ When the device is kept in low power standby mode, the JTAG ports: TMS\TDI and TDO must be set low, and TCK must stop working (either high or low).

After configuration is complete, use the FPGA DONE signal to drive the

PROM $\overline{CE}$ If the DONE pin is high to reduce standby power consumption, an external pull-up resistor is required. A 330 Ω pull-up resistor is generally used. The pull-up resistor value of the DONE port needs to be checked in the FPGA data file. If the DONE circuit is connected to an LED to indicate that the configuration is complete, it must also be connected to the PROM. $OE/\overline{RESET}$ To enable power saving sleep mode, however, an external buffer is required to drive the LED circuit to ensure the correct transition to the PROM $\overline{CE}$ If the PROM does not require low-power sleep mode, then $OE/\overline{RESET}$ Should be grounded.

The following table is the input control truth table of PROM:

Table 5. BST16P input control truth table

Input control signal				Internal Address	Output			
$OE/\overline{RESET}$	$OE/\overline{RESET}$	$\overline{CE}$	BUSY(5)		DATA	$\overline{CE}$	CLKOUT	ICC

high	Low	high	Low	If address < TC(2) and < EA(3): increase	activation	high	activation	activation
				If address < TC and = EA: unchanged	High resistance	high	High resistance	reduce
				If address = TC: unchanged	High resistance	Low	High resistance	reduce
high	Low	high	high	constant	Activation and invariance	high	activation	activation
high	Low	↑	X(1)	Reset(4)	activation	high	activation	activation
Low	Low	X	X	Keep Reset	High resistance	high	High resistance	activation
X	high	X	X	Keep Reset	High resistance	high	High resistance	Hibernation

Note:

- X=any value.
- TC: Final count, end address value.
- BST16P design version is valid, EA: the end address of the selected version.
- BST16P design version is valid, reset: the address is reset to the initial address of the selected module. If the design version is invalid, the reset address is reset to 0.
- The BUSY input is only valid when the BST16P is outputting data in parallel and decompression is disabled.

XXI. Detailed Functional Description

BST16P is a 16Mbits FPGA configuration memory compatible with Xilinx ISE software, supporting four FPGA configuration modes: master-serial, slave-serial, master-parallel,

and slave-parallel.

- JTAG

The BST16P Flash RPOMs platform supports the IEEE 1149.1 boundary scan standard and the IEEE 1532 online configuration standard. The test access interface (TAP) and registers are used to support boundary scan instructions and optional special IEEE 1149.1 standard instructions. In addition, the connection of the PROM TAP makes online programming (ISP), configuration, erase and verification operations more convenient. Table 11 lists the required and optional boundary scan instructions for the Flash PROM platform. The boundary scan structure and the required optional instructions can be completed according to the IEEE 1149.1 standard specification.

Table 6. BST16P boundary scan instructions

Boundary Scan Instructions	BST16P IR[15:0]	Instruction Description
Required instructions		
BYPASS	FFFF	Enabling BYPASS
SAMPLE/PRELOAD	0001	Enable boundary scan SAMPLE/PRELOAD operation
EXTEST	0000	Enable boundary scan EXTEST operation
Optional instructions		
CLAMP	00FA	Enable boundary scan CLAMP operation
HIGHZ	00FC	Set all outputs to high impedance at the same time
IDCODE	00FE	Enable shifting out 32-bit IDCODE
USERCODE	00FD	Enable shifting out 32-bit USERCODE
Flash RPOM special instructions		
CONFIG	00EE	pass $\overline{CF}$ Initialize FPGA to low

When the BYPASS instruction is valid, the BYPASS register is a one-bit register

connected directly from TDI to TDO. In the CAPTURE-DR state, the BYPASS register is downloaded to logic 0 on each TCK rising edge.

The boundary scan registers can be used to control and observe the state of the port during EXTEST, SAMPLE/PRELOAD and CLAMP instructions. Each output port of the Flash PROM has two registers for boundary scan, while each input port has only one register. Bidirectional ports have three boundary scan registers. For each output port, the register closest to TDI controls and observes the output state, and the register next to TDO controls and observes the high-impedance enable state of the output port. For each input port, a separate register controls and observes the input state of the port. Bidirectional ports contain three bits, the first input bit, the second output bit, and the last output enable bit. The output enable bit is closest to TDO. The boundary scan bits and order of all connected device ports will be introduced later in the I/O. In the boundary scan register, the boundary scan cell is set to 0 as the LSB, which is the register closest to TDO.

- TAP

The Flash PROM family can simultaneously perform in-circuit programming and IEEE1149.1 boundary scan testing (JTAG) with a single 4-wire test access interface (TAP). This simplified system allows standard automatic test equipment to perform both functions simultaneously. The AC features of the Flash PROM TAP platform are described below.

- TAP Controller

The following figure shows the 16-bit state controller of BST16P. The four TAP ports control the data to be scanned and moved into various registers. At each rising edge of TCK, TMS determines the state transfer timing. There are two main timing relationships here: one is to move data into the data register, and the other is to move instructions into the instruction register.

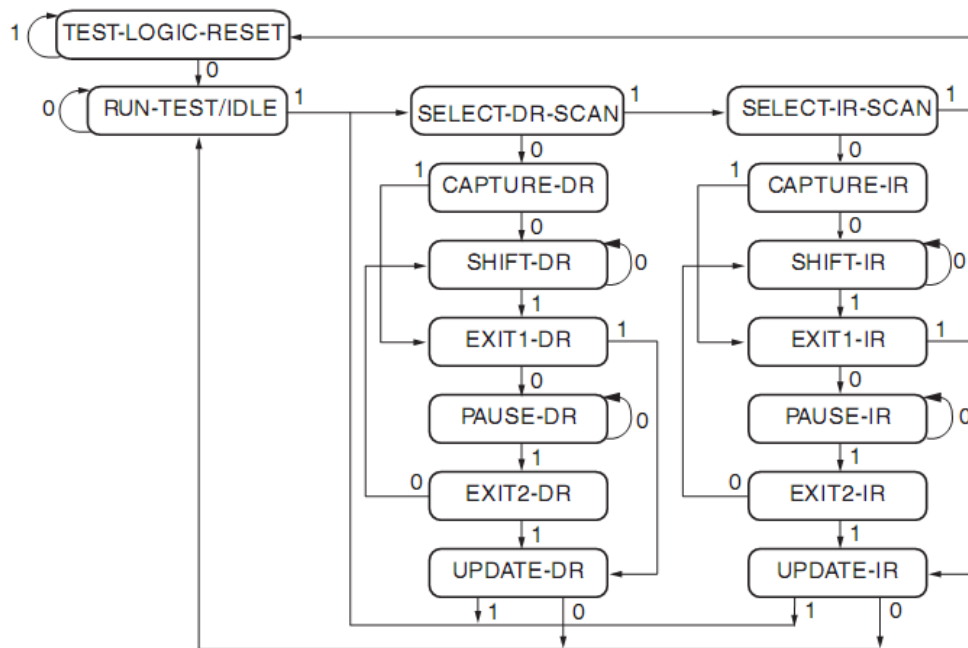


Figure 7. 16-bit state machine

- IDCODE Register

IDCODE is fixed and used for manufacturer identification and address identification of special devices. The IDCODE register has a width of 32 bits. The IDCODE shift register can be shifted out and checked by using the IDCODE instruction.

Table 7. IDCODES of BST16P

Devices	IDCODE(1)(hex)
BST16P	<v>5058093

Note:

The <v> in IDCODE represents the variable code of the device.

The IDCODE register uses the following binary mode:

VVVV: FFFF: FFFF: AAAA: AAAA: CCCC: CCCC: CCC1

V: is a fixed version number.

F: PROM family code.

A: ID of special Flash PROM product.

C: ID of the process manufacturer.

The LSB of the IDCODE register is defined as 1 according to IEEE Standard 1149.1.

- **USERCODE Register**

Allows access to the 32-bit user programmable USERCODE instruction, which is used to provide information about device programming. By using the USERCODE instruction, the user programmable verification code can be checked and removed. During Flash PROM platform programming, the code is downloaded into the USERCODE register. If the period is blank or not downloaded during programming, the USERCODE register is FFFFFFFFh.

- **Instruction Register**

The instruction register of the Flash PROM platform is connected during the instruction scan. TDI and TDO are connected. In preparation for the instruction sequence scan, the instruction register is loaded with fixed instructions in parallel to obtain the mode. When an instruction is moved into the instruction register from TDI, this mode will be moved out first by TDO.

During the instruction sequence scan, the BST16P PROM's sixteen-bit wide instruction register (IR) is connected between TDI and TDO.

Table 8. BST16P reads the command value of the IR register

TDI →	IR[15:9]	IR[8:7]	IR[6:5]	IR[4]	IR[3]	IR[2]	IR[1:0]	→ TDO
	Reserved	ISC Error	ER/PROG Error	ER/PROG Status	ISC Status	DONE	0 1	

The BST16P device shifts out the mode obtained by IR[15:0]. IR[15:9] are

reserved bits. IR[8:7] are ISC right or wrong status, which is 10 when the ISC operation is successful; on the contrary, it is 01 when the ISC online configuration fails. IR[6:5] are the erase/program success status, which is 10 when the erase or program is successful; on the contrary, it is 01 when the erase or program fails. IR[4] is the erase/program status, which is 0 when the device is working in the erase or program operation; on the contrary, it is 1. IR[3] ISC status, which is 1 if it is currently in online configuration mode; on the contrary, it is 0. IR[2] is the DONE status, which is 1 if the example design version is successfully programmed; logic 0 indicates that programming is not completed. The remaining IR[1:0] are set to 01 according to IEEE Standard 1149.1.

- Internal crystal

The BST16P has an internal selectable crystal that can be used to drive CLKOUT and the FPGA configuration connections. When programming the PROM, the internal crystal can be enabled and can be set to a default or lower operating frequency.

- CLKOUT

The BST16P has a programmable option to enable the CLKOUT signal, which is a synchronous clock source that enables the data on the configuration connection to be arranged in order. The CLKOUT signal can come from the CLK input port or the internal oscillator. The input clock source is valid during PROM programming, and data is validly output on the rising edge of CLKOUT.

During programming, the CLKOUT signal is activated. $\overline{CE}$ Go low, $\overline{OE}/\overline{RESET}$ is

high. $\overline{EN}_{EXTSEL}$ When the rising edge jumps, if $\overline{CF}$ If the PROM terminal count is not reached, CLKOUT remains active for eight clocks before it is invalid. When CLKOUT is invalid, the CLKOUT port is set to a high impedance state or may be

pulled up externally to a fixed state.

When the CLKOUT of the cascaded Flash PROM platform is valid, after the first PROM data transfer is completed, the first CLKOUT becomes invalid and drives $\overline{CE}$ enables the next PROM in the cascade. Once the next PROM is valid and data is allowed to transfer, its CLKOUT signal will be driven.

- Unzip

The 16Mb BST16P Flash PROM platform has a built-in hardware data decompression module compatible with the latest Xilinx compression technology. Flash PROM compressed files are FPGA bitstreams compressed by IMPACT software. Only slave-serial and slave-parallel configuration modes support compressed bitstream configuration of FPGA.

During PROM programming, when the decompression option is enabled, the PROM decompresses the data before driving the clock and data to the configuration connection of the FPGA. If decompression is enabled, the Flash clock output port (CLKOUT) must be used as the clock signal for the configuration connection and drive the configuration clock (CCLK) of the target FPGA device. The PROM's CLK input or internal oscillator can be used as the CLKOUT clock source. In the configuration chain, any FPGA connected to the PROM must be in slave serial or slave parallel configuration mode.

When decompression is valid, the CLKOUT signal is a maximum frequency control clock. When decompression data is not ready, the CLKOUT signal will be high impedance or pulled up to a certain state. When decompression is valid, the BUSY input will automatically be invalid.

- Design version

Design version technology allows users to store up to four design versions in a

single PROM or multiple PROM cascade designs. The 16Mb BST16P Flash PROM platform supports design version technology in both serial and parallel modes. When CLKOUT is valid, the design version can be compressed using the PROM file. When using iMPACT software, a programmable PROM file (.cfi) with version information is created. This requires the use of a .cfi file to make the design version valid during iMPACT software programming.

A single design version requires 1 to n 8Mb memory blocks. If a single design version contains less than 8Mb of data, the remaining space will be set to all 1s. A large design version can use multiple 8Mb memory blocks, and the remaining space of the final 8Mb memory block will be set to all 1s. Because at least 8Mb of space is required for each version, a 16Mb PROM can only have a maximum of two independent design versions: one 16Mb design version, one 8Mb design version, or two 8Mb design versions. Larger design versions can be achieved by using multiple cascaded PROMs. See Figure 10 for a basic example of multiple storage versions. Design versions can be obtained during the use of iMPACT.

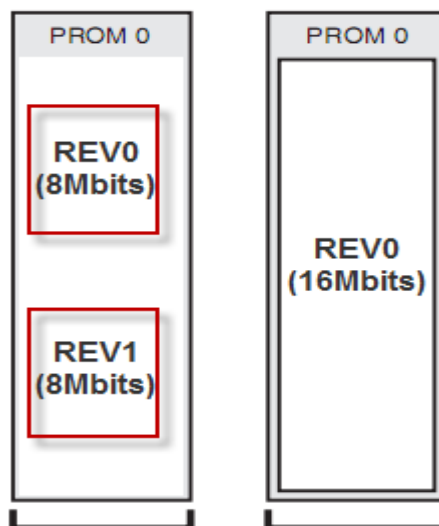


Figure 8. Multiple storage version examples

During PROM file generation, each design revision is set to the following values:

- Revision 0 = '00'
- Revision 1 = '01'

After the Flash PROM platform containing the design version is programmed, an independent design version can be selected through the external REV_SEL[1:0] or the internal programmable design version control bit. $\overline{OE}/\overline{RESET}$ The port determines the external port or internal bit to select the design version. $\overline{CF}$ When it is low, the design version is determined by the external port REV_SEL[1:0]. $\overline{CE}$ When high, the design revision is determined by the internal programmable control bit selection. During power-up, the design revision select input (port or control bit) is sampled internally. After power-up, the design revision select input will be sampled again when the following conditions occur:

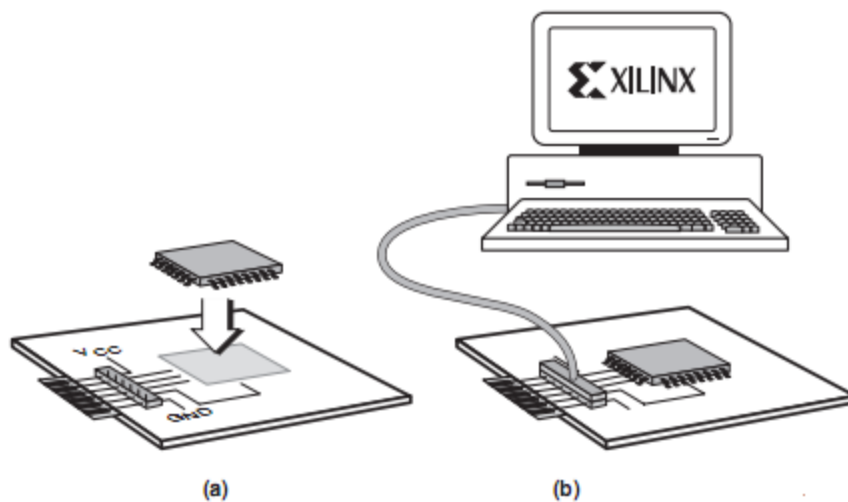
- $\overline{OE}/\overline{RESET}$ Generate rising edge
- $\overline{CF}$ Generates a falling edge ($\overline{CE}$ is low)
- When reconfiguring using the JTAG CONFIG instruction

The configuration data of the selected design version will appear at the FPGA configuration connection.

XXII. Application Notes

The online programmable PROM can be programmed individually or in two or more cascaded rings through the standard four JTAG protocol ports (as shown below). Online programming provides a fast and efficient design cycle, eliminating unnecessary packaging operations and device sockets. Design data can be sequentially transferred to the device through Xilinx iMPACT software and Xilinx download cables, a third-party JTAG

development system, a JTAG-compatible test board, or a microprocessor that emulates the JTAG instruction sequence. iMPACT software can also output any svf file format that supports serial vector (svf) tools, including automatic test equipment. During online programming, $\overline{CF}$ Output is high, all other outputs are fixed in high impedance state or clamped at a certain level. In-circuit programmable will fully support the recommended industrial voltage and temperature variations.



(a) Soldering the device to the PCB (b) Using a programmable download cable

Figure 9. JTAG online programming operation

In a traditional industrial environment, a third-party programmer can program the PROM before it is assembled on the board. Information on Flash PROM platform support can be obtained by contacting a preferred third party.

BST16P online programmable products guarantee 20,000 program/erase cycles and a minimum retention time of 20 years. Within this effective limit, all functions, operating conditions and data parameters of each device can be referred to this parameter manual.

The BST16P In-Circuit Programmable Flash PROM device platform incorporates the latest

data security features to prevent FPGA data from being read by unauthorized JTAG or inadvertently written by JTAG. Table 10 shows the respective security settings for the BST16P PROM.

Table 9. BST16P version data security settings

Read protection	Write protection	Anti-read/verification	Anti-programming	Anti-erasure
Reset (Default)	Reset (Default)	-	-	-
Reset (Default)	Setting effective	-	√	√
Setting effective	Reset (Default)	√	-	-
Setting effective	Setting effective	√	√	√

The user can design a read protection security bit to prevent the internal programming template from being read or copied by JTAG. Read protection does not hinder write operations. The read protection security bit of BST16P PROM can be set for the design version separately. To reset the read protection bit, you need to erase part of the design version.

The BST16P PROM device also allows write protection for a specific design version or as an optional setting of the PROM. Write protection prevents an inadvertent JTAG instruction from modifying/erasing the protected area. The write protection setting can be cleared by erasing the protected area. However, the XSC_UNLOCK instruction must be entered into the BST16P PROM before the ISC_ERASE instruction to unlock it. The XSC_UNLOCK and ISC_ERASE instructions can be found in the BST16P PROM BSTL file.

Note:

When iMPACT software performs an erase operation on the BST16P PROM, the XSC_UNLOCK problem is often encountered. This is usually because the write protection is not unlocked.

- Main String Mode

In master serial mode, the FPGA will automatically and synchronously download the bit stream from the external bit serially for configuration according to the internally generated clock CCLK. When powered on or reconfigured, the FPGA mode select port will select the master serial configuration mode. The master serial mode provides a simple configuration connection. When configuring the FPGA, only a serial data line, a clock line, and two control lines (INIT and DONE) are required. As the PROM internal address counter increases with each valid rising edge of CCLK, the configuration data is read out in order from a single data line (DIN). A short period of time before each rising edge of the FPGA internal clock signal CCLK, the serial bit stream data must be established at the DIN input port of the FPGA.

- Slave Serial Mode

In slave-serial mode, the FPGA will automatically and synchronously download the configuration bit stream from the external bit serially according to the external clock. When powered on or reconfigured, the FPGA mode select port will select the slave-serial configuration mode. The slave-serial mode provides a simple configuration connection. When configuring the FPGA, only a serial data line, a clock line, and two control lines (INIT and DONE) are required. With each valid rising edge of CCLK, the PROM internal address counter increases, and the configuration data is read out in order from a single data line (DIN). A short period of time before each rising edge of the external clock signal CCLK, the serial bit stream data must be established at the DIN input port of the FPGA.

- Cascade Mode

Cascading PROMs provide additional storage when configuring multiple FPGAs in a serial ring, configuring multiple FPGAs in a parallel chain, or configuring an FPGA that requires a larger bitstream. Multiple Flash PROMs can be connected through

the previous device $\overline{OE}/\overline{RESET}$ Output to drive the next device $\overline{OE}/\overline{RESET}$. In the chain, the clock signals and data outputs of all Flash PROMs are interconnected.

When the last data of the first PROM is read out, the first PROM will declare $\overline{CEO}$.

The second PROM recognizes that $\overline{OE}/\overline{RESET}$ is a low input immediately makes its output valid.

After configuration is complete, if the PROM $\overline{OE}/\overline{RESET}$ is Low or $\overline{OE}/\overline{RESET}$ is high, all cascaded PROM address counters are reset.

When the PROM is the master, the CLKOUT of the PROM must be connected to the CCLK port of the FPGA; BUSY needs to change on the falling edge of the clock.

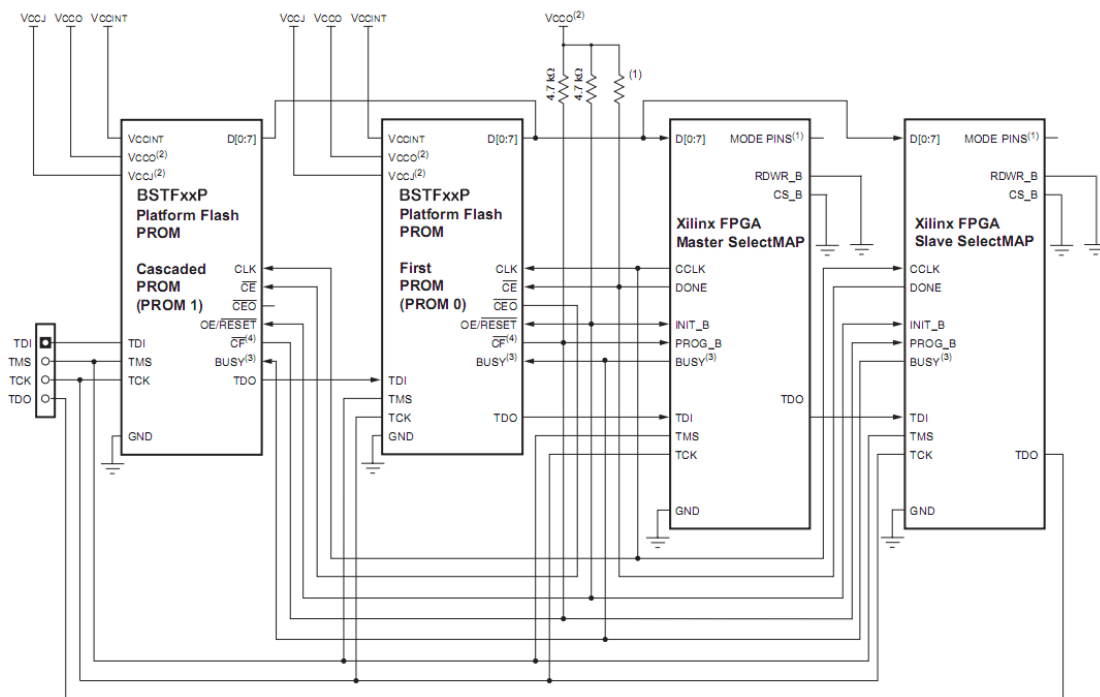


Figure 10. Configuring multiple chips using a master/slave parallel mode

Note:

- For the connections of the mode port and the pull-up value of the DONE port,

refer to the appropriate FPGA data sheet or the user configuration help documentation for the FPGA family.

- For compatible voltage values, please refer to the relevant data sheet.
- The BUSY port is only in the BST16P Flash PROM. (The BUSY port connection is required only when the FPGA series is configured in high-frequency parallel mode). If there is no BUSY port in the FPGA or the BUSY port is not required when configuring the device, the PROM BUSY port is not connected or grounded. For detailed information about the BUSY port, refer to the relevant FPGA data manual or FPGA configuration help document.

BST16P $\overline{PCF}$ For bidirectional ports. In BST16P, if $\overline{PROGRAM}$ If not connected to $\overline{PROG_B}$, $\overline{CF}$ Must be connected to VCCO through a 4.7K Ω pull-up resistor.

XXIII. Precautions

- Power-on sequence requirements: VCCINT is powered on first, and VCCO is powered on later. (See switch characteristics for details)
- Because the BST16P chip $\overline{CF}$ The falling edge of the pin is sensitive. If the system board has a lot of interference, it is easy to cause the BST16P to not output data. $\overline{CF}$ Then release it to high, so that BST16P can output data again. It is recommended that users make the following design when designing the board to reduce $\overline{CF}$ Glitches on the pins, thus avoiding this anomaly:
 - Modify the system board $\overline{CF}$ The pull-up resistor is 1K Ω resistor;
 - In $\overline{CF}$ Connect a 1nf capacitor between GND and the

XXIV. Package Specifications

The device adopts ceramic sealed FBGA48 lead-out terminals, and its dimensions refer to the provisions of GB/T 7092-1993. The outer shell shape is shown in Figure 11.

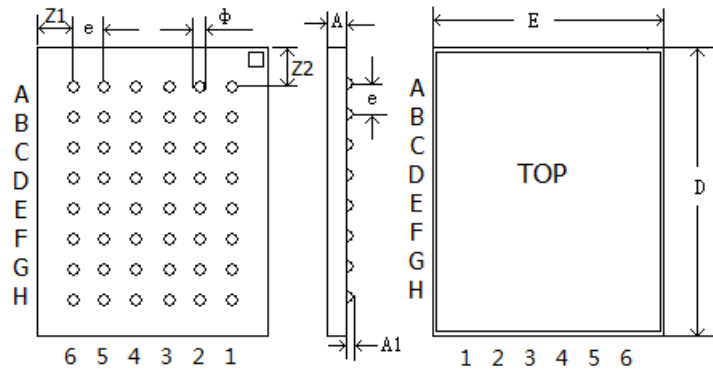


Figure 11. Dimensions

Unit is mm

Dimension symbols	Numeric		
	Minimum	Nominal	maximum
D	8.80	-	9.20
E	7.80	-	8.20
A	-	-	2.15
A1	0.40	-	0.60
e	-	0.80	-
Z1	1.85	-	2.15
Z2	1.55	-	1.85
φ	0.35	-	0.48

XXV. Ordering Information

model	Package	Pack- age Type	External pins	Quality Grade	General Specifica- tions	Detailed specifi- cation number	Prod- uct Status
BST16PMHM	CFBGA48	Her- metic pack- aging	Solder ball Sn10Pb90 Solder Paste Sn63Pb37	Class B	GJB597B- 2012	Q/BST 20151- 2013	Mass pro- duction