BST16D250

1. Product Overview

BST16D250 It is a dual-channel, 16-bit, high dynamic range DAC that supports up to 250Msps The conversion rate can output multi-carrier broadband signals within the Nyquist band. The internal design is specifically designed for direct conversion transmission applications, including gain and offset compensation. The DAC output can be seamlessly connected to an analog quadrature modulator. Use 4 SPI Interface, can be used for DAC Perform configuration, reading, etc. The DAC output current can be configured from 8.6mA to 31.7mA.

Product Advantages

1. Low noise, low harmonics, and low intermodulation distortion (IMD), capable of outputting high-quality broadband signals.
2. High Nyquist zone analog output capability (mixer mode).

Programmable differential output current capability from 8.6mA to 31.7m a.

Characteristic

- High dynamic range, dual DACs with low noise and intermodulation distortion.
- Single Carrier WCDMA ACLR=80dBc@61.44MHz IF.
- Support high Nyquist frequency output capability.
- Dual or single port interleaved LVCMOS data input interface 8.6mA to 31.7mA programmable differential output current.
- 10-bit auxiliary DAC supports external analog signal bias adjustment Built-in 1.2v precision bias.
- 1.8v and 3.3v power supply.
- 4-wire SPI control interface.
- 310mw typical power consumption.
- 72-pin QFN package.
- -40 °C ~ +85 °C operating temperature range.

2. Functional Block Diagram

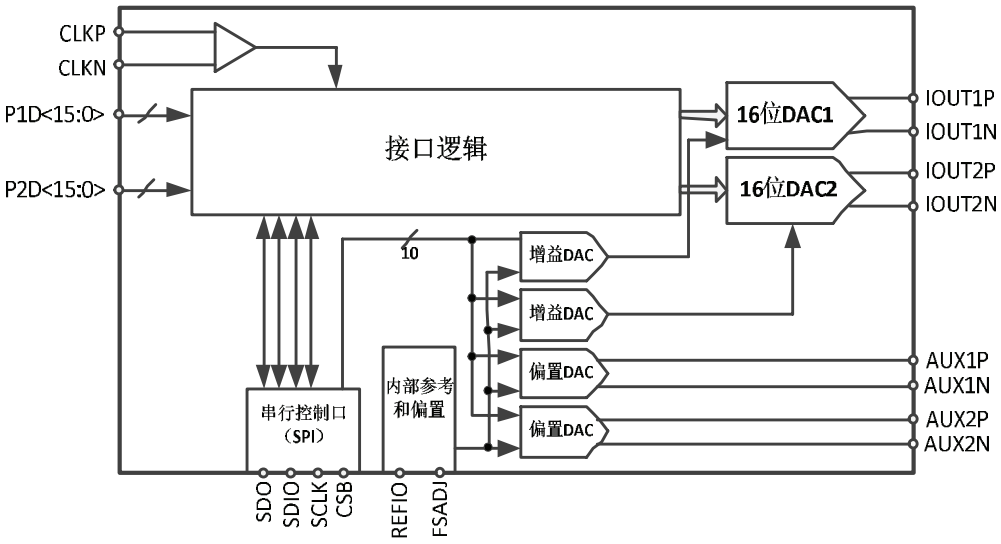

Figure 1. BST16D250 Functional Block Diagram

3. Electrical Parameters

DC Specifications

Unless otherwise noted, test conditions: AVDD33 = 3.3 V, DVDD18 = CVDD18 = 1.8 V, I_{FS} = 20 mA, Full Power Digital Input, f_{DAC} = 250Msps.

Table 1

Parameter	Minimum	Typical Value	Maximum	Unit
Resolution		16		Bit
Accuracy				
Integral Nonlinearity (INL)		±2.0		LSB
Differential Nonlinearity (DNL)		±4.0		LSB
DAC analog output				
Offset Error		±0.001		% FSR
Gain Error (Using Internal Reference)		±2.0		% FSR
Full scale output current	8.6		31.7	mA
Output voltage range	- 1.0		+1.0	V
Output Impedance		10		MΩ
Auxiliary DAC input and output				
Resolution		10		Bit
Full scale output current	- 2.0		+2.0	mA
Full Output Voltage Range – Current Sink Mode	0.8		1.6	V
Full Output Voltage Range – Source Current Mode	0		1.6	V
Input or output impedance		1		MΩ
DAC Temperature Drift				
Gain	100	ppm /°C		
Offset Error	0.1	ppm /°C		
Reference voltage	10	ppm /°C		
Reference source				
Internal reference voltage		1.2		V
External input range	1.15		1.3	V
Output Impedance		5		kΩ
Analog supply voltage				
AVDD33	3.13	3.3	3.47	V
CVDD18	1.70	1.8	1.90	V
Digital supply voltage				
DVDD33	3.13	3.3	3.47	V
DVDD18	1.70	1.8	1.90	V
Supply current				
IAVDD33		57	62	mA
IDVDD33		12	17	mA
ICVDD18		19	23	mA
IDVDD18		33	37	mA

Digital specifications

Unless otherwise noted, test conditions: AVDD33 = 3.3 V, DVDD18 = CVDD18 = 1.8 V, I_{FS} = 20 mA, Full Power Digital Input, f_{DAC} = 250Msps.

Table 2

Parameter	Minimum	Typical Value	Maximum	Unit
LVCMOS data input				
Input high voltage	2.0			V
Input low voltage			0.8	V
Input Current			1	uA
Data to DAC clock setup time (t DBS Dual-port mode)	400			ps
Data to DAC Clock Hold Time (tDBH Dual-port mode)	1200			ps
Pipeline delay (dual-port mode)			7	Clock cycle
Data or IQSEL input to DAC clock setup time (t DBS Single port mode)	400			ps
Data or IQSEL input to DAC clock hold time (t DBS Single port mode)	1200			ps
Pipeline delay (single-port mode)			8	Clock cycle
DAC clock input (CLKP, CLKN)				
Differential Peak-to-Peak	400	800	1600	mV
Single-ended peak-to-peak			800	mV
Common mode voltage	300	400	500	mV
Input Current			1	uA
Clock frequency			250	MHz
DAC Clock Output (DCO)				
Output high voltage	2.4			V
Output low voltage			0.4	V
Output Current			10	mA
DAC Clock to DCO Delay (t_{DCO})	2.0	2.2	2.8	ns
SPI interface				
Clock frequency (f_{SCLK})			40	MHz
Minimum pulse width				
High level (t_{PWH})	10			ns
Low level (t_{PWL})	10			ns
SDIO to SCLK setup time (t_{DS})	1			ns
SDIO to SCLK hold time (t_{DH})	0			ns
CSB to SCLK setup time (t_{DCSB})	1			ns
CSB to SCLK hold time (t_{DCSB})	0			ns
SCLK to SDIO/SDO data valid time (t_{DV})			1	ns
RESET high pulse width	10			ns

AC Specifications

Unless otherwise noted, test conditions: AVDD33 = 3.3 V, DVDD18 = CVDD18 = 1.8 V, I_{FS} = 20 mA, Full Power Digital Input, f_{DAC} = 250Msps.

Table 3

Parameter	Minimum	Typical Value	Maximum	Unit
Spurious Free Dynamic Range (SFDR)				
f_{DAC} = 250MSPS, f_{OUT} = 20MHz		80		dBc
f_{DAC} = 250MSPS, f_{OUT} = 70MHz		70		dBc
f_{DAC} = 250MSPS, f_{OUT} = 180MHz (Note 1)		65		dBc
Intermodulation distortion (IMD)				
f_{DAC} = 250MSPS, f_{OUT} = 20MHz		84		dBc
f_{DAC}=250MSPS, f_{OUT}=70MHz		80		dBc
f_{DAC}=250MSPS, f_{OUT}=180MHz (Note 1)		72		dBc
Crosstalk				
f_{DAC}=250MSPS, f_{OUT}=20MHz		80		dBc
f_{DAC}=250MSPS, f_{OUT}=70MHz		80		dBc
f_{DAC}=250MSPS, f_{OUT}=180MHz (Note 1)		80		dBc
Noise Spectral Density (NSD)				
f_{DAC} =250MSPS, f_{OUT} =15.36MHz		- 164		dBm /Hz
f_{DAC} =250MSPS, f_{OUT} =61.44MHz		- 161		dBm /Hz
f_{DAC} = 250MSPS, f_{OUT} = 184.32MHz (Note 1)		- 159		dBm /Hz

Note 1: Working in Mixer Mode