BST1472CPLD
Product Brochure

Product Overview

BST1472 is a high-density, high-performance complex programmable logic device (CPLD) based on the "product term" principle, with 1600 available gates; the core power supply voltage is 3.3V/5V, the I/O voltage is 3.3V/5V; the number of logic arrays (FB) is 4, with 72 trigger resources; the operating temperature range is -55℃～+125℃, the maximum Pin-to-Pin delay time is 10ns, and the maximum system frequency is 111MHz; ESD protection is not less than 4000V.

Table 1Basic product information

Product Model	BST1472		
Package	CLCC44 (Ceramic)	CQFP44 (ceramic)	VQFP44 (Plastic)
Quality Assurance Level	B-level	B-level	PQFP100N (Plastic) Grade
Available IO number	34	34	N34
Macrocell	72		81
Available doors	1600		
TPD(ns)	10		
FCNT(MHz)	111		

Product Features

- 5V in-system programming capability based on IEEE Std.1149.1JTAG protocol;
- Compatible with Xilinx burning software IMPACT to perform JTAG operations on the chip;

- The core power supply voltage is 5V/3.3V, and the IO voltage is 5V/3.3V;
- Maximum pin delay of 10ns;
- The 16-bit counter frequency Fcnt (same FB) can reach up to 111Mhz;
- In the same FB, 90 Product Terms can drive any macro cell (MC);
- The power consumption mode of each macro cell can be independently programmed to reduce its power consumption by 20% or more;
- Each output can configure its slew rate;
- Support hot-swap;
- ESD protection is greater than or equal to 4000V;
- Macrocell registers can be programmed for independent clear, set, clock, and clock enable control;
- Programmable device encryption bits protect user designs;
- It has three invertible global clocks;
- Unconfigured pins can be configured to be grounded;
- Applications:
- These devices are widely used in applications such as bus bridging, I/O expansion, power-on reset (POR), timing control, and device initialization control.

Functional Block Diagram

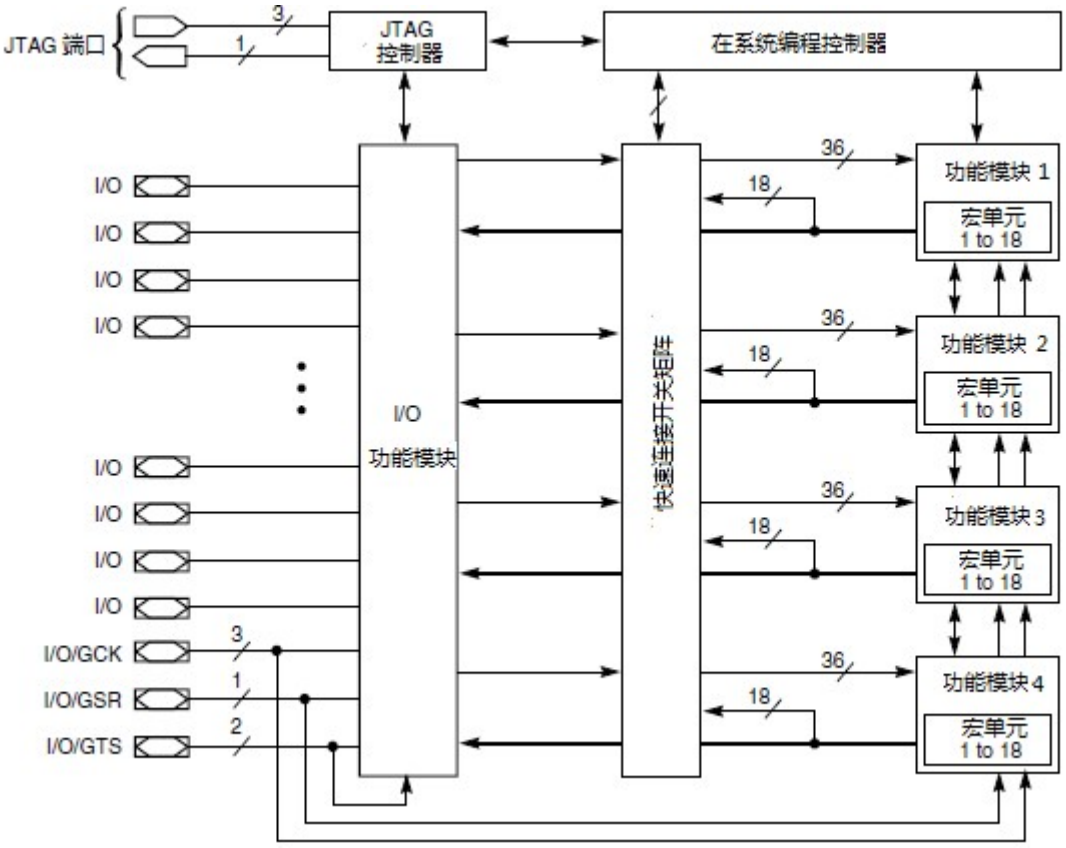

Figure 1 BST1472 block diagram