

BST1258

1. Product Overview

BST1258 It is a 16-channel single-loop fixed data transmitter that can provide channel scan rates from 1.8Ksps to 23.7ksps (multiplexed) , low noise, 24 -bit, delta-sigma ($\Delta\Sigma$) analog-to-digital converter (ADC). Its differential flexible input selector can accept 8 differential inputs or 16 single-ended inputs with a 5V full-scale differential range or $\pm 2.5V$ bipolar range under a 5V reference. A 4th-order $\Delta\Sigma$ modulator and a subsequent 5th-order sinc digital filter are used to optimize the circuit's low noise characteristics.

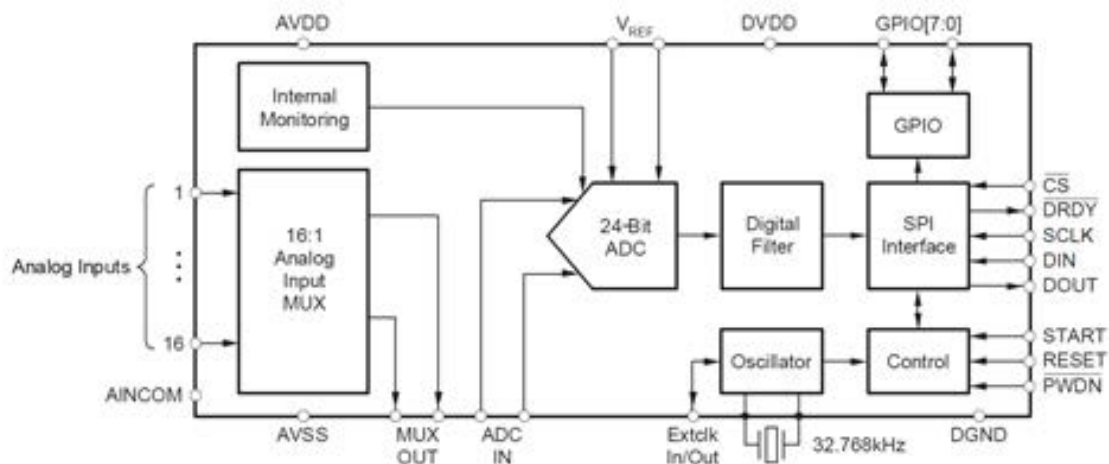
The multiplexer differential outputs can be connected to a signal conditioner before being connected to the ADC inputs. Internal system monitoring registers provide data on supply voltage, temperature, reference voltage, gain error, and offset.

The system clock can be based on an on-chip phase-locked loop based on a 32.768kHz crystal oscillator or an external clock source.

(15.7MHz) output can drive a microcontroller or additional converter.

The internal interface is compatible with serial data exchangers. Simple instruction set controls channel configuration, data rate, digital I/O, monitor functions, etc.

Programmable sensor bias current sources can be used to bias the sensor or modulate sensor integrity. BST1258 is unipolar + 5V or bipolar $\pm 2.5V$, and the digital power supply voltage is compatible with the interface voltage of 2.7V to 5.25V. BST1258 adopts CLCC-48 package.



2. Product Features

- 24 bits, no missing code.
- Fixed channel or automatic channel scanning.
- Fixed channel data rate: 125kSPS.
- Automatic channel scanning data rate: 23.7kSPS /channel.
- Single conversion fixed data.
- 16 unidirectional or 8 differential inputs.
- Unipolar (+5V) or bipolar ($\pm 2.5V$) operating voltage.
- Low noise: 2.8 μ Vrms at 1.8kSPS.
- 0.0003 % integral nonlinearity.
- DC stability characteristics: 0.02 μ V/ $^{\circ}$ C offset drift, 0.4ppm/ $^{\circ}$ C gain drift.
- Open sensor detection.
- Conversion control (pin or command).
- Multiplexer output for external signal conditioning.
- On-chip temperature, impedance, offset, gain, voltage input readback.
- Power consumption: 42mW
- Standby, sleep, and power saving modes
- 8 general purpose input and output interfaces (GPIO)
- 32.768kHz crystal or external clock.

3. Functional Block Diagram

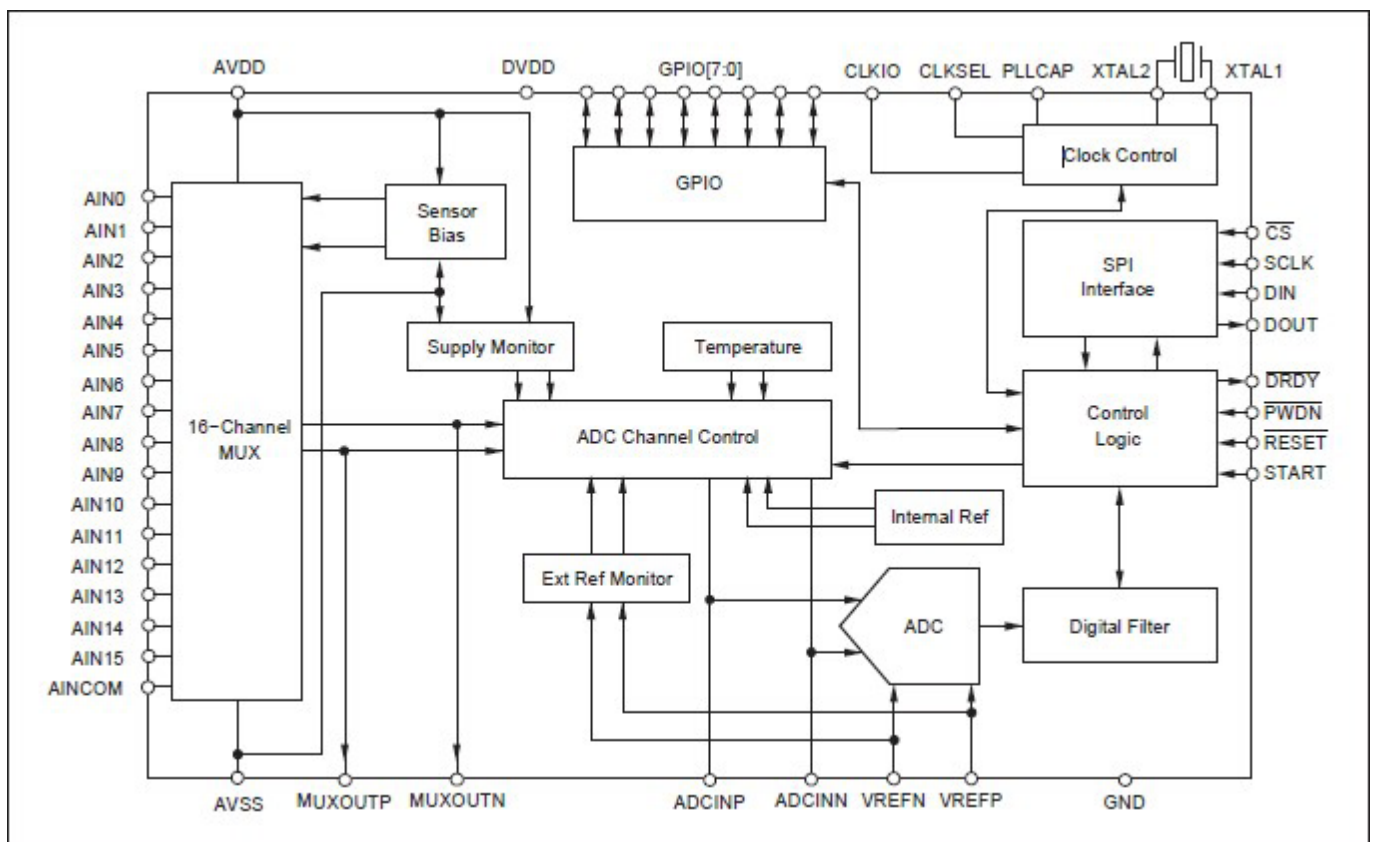


Fig.1. BST1258 block diagram

4. Electrical Parameters

All specifications are for $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $AVDD = +2.5\text{V}$, $DVDD = +3.3\text{V}$, $V_{REF} = +4.096\text{V}$, $V_{REFN} = -2.5\text{V}$,
 $f_{CLK} = 16\text{MHz}$ (external clock) or $f_{CLK} = 15.729\text{MHz}$ (internal clock), the OPA 227 buffer is connected between the MUX output and Between ADC inputs, unless otherwise specified

Table 1

Parameter		Test conditions	BST1258			Unit
			Minimum	Typical Value	Maximum	
Analog multiplexer input						
Absolute input voltage	AIN0- AIN15, AINCOM Recom- mended DGND		AVSS -100mV		AVDD+100mV	V
Channel resistance				80		Ω
Crosstalk		fIN = 1kHz		-110		dB
Sensor bias (current source)		SBCS[1:0]=01		1.5		μA
		SBCS[1:0]=11		24		
1.5μA: 24μA Proportional Error				1		%
ADC enter						
Full range input voltage Pressure	(VIN = ADCINP-ADCINN)			±1.06V REF		V
Absolute input voltage	(ADCINP, ADCINN)		AVSS-100mV		AVDD+100mV	V
Differential input impedance				65		KΩ
System Performance						
Accuracy		No missing codes	24			Bits
Data rate, fixed channel mode			1.953		125	SPS
Data rate, automatic scanning mode			1.805		23.739	SPS
Integral Nonlinearity (INL) ⁽¹⁾		Differential input		0.0003	0.0010	%ofFSR ⁽²⁾
Offset Error	Chopping off	Input short circuit		20		μV
	Chopping On			1	10	
Offset Drift	Chopping off	Input short circuit		0.5		μV/°C
	Chopping On			0.02	0.1	
Gain Error				0.1	0.5	%
Gain Drift				0.4	2	ppm/°C
noise			(See Table 6)			
Common Mode Rejection		fCM = 60Hz	90	100		dB
Power Supply Rejection	AVDD,AVSS	fPS = 60Hz	70	85		dB
	DVDD		80	95		
Reference voltage input						
Reference input voltage	(VREF = VREFP-VREFN)		0.5	4.096	AVDD- AVSS	V
Negative Reference Input (VREFN)			AVSS - 0.1V		VRERP -0.5	V
Positive reference input (VREFP)			VREFN+0.5		AVDD+0.1V	V
Reference voltage input impedance				40		kΩ

(1) The best linear method

(2) FSR = Full Scale Range = $2.13V_{REF}$

(3) Ensure characteristics

(4) Only BST1258 temperature setting, test PCB board at natural temperature

(5) BST1258 and test PCB board temperature are set together

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Table 2

Parameter		Test conditions	BST1258			Unit
			Minimum	Typical Value	Maximum	
System Parameters						
External reference reading error				1	3	%
Analog power reading error				1	3	%
Temperature sensor reading	Voltage	TA = +25°C ⁽⁴⁾		168		mV
	coefficient	See note ⁽⁴⁾		394		μV/°C
		See note ⁽⁵⁾		563		μV/°C
Digital Input/Output						
Logic Level	V _I		0.7DVDD		DVDD	V
	V _{IL}		DGND		0.3DVDD	V
	V	I _{OH} = 2mA	0.8DVDD		DVDD	V
	V _{OL}	I _{OL} =2mA	DGND		0.2DVDD	V
Input leakage current		V _{IN} =DGND,GND			10	μV
Master clock input (CLKIO)	frequency		0.1		16	MHz
	Duty Cycle		40		60	%
Crystal oscillator (see the crystal oscillator section)	Crystal frequency			32.768		kHz
	Clock output frequency			15.729		MHz
	Start-up time (clock available input out)			150		ms
	Clock output duty cycle		40		60	%
power supply						
DVDD			2.7		5.25	V
AVSS			- 2.6		0	V
AVDD			AVSS+4.75		AVSS+5.25	V
DVDD supply current	External clock operation			0.25	0.6	mA
	Internal clock working, clock no input out			0.04		mA
	The internal clock is working and the clock has input Out ⁽⁶⁾			1.4		mA
	Power failure ⁽⁷⁾			1	25	μA
AVDD,AVSS power supply flow	Conversion			8.2	12	mA
	Standby			5.6		mA
	Sleep			2.1		mA
	Power off			2	85	μA
Power consumption	Conversion			42	62	mW
	Standby			29		mW
	Sleep			11		mW
	Power off			14		mW

(6) CLKIO load = 20pF

(7) No clock is supplied to CLKIO

5. Ordering Information

Product Model	Quality Grade	Package	Packaging materials
BST1258-A	B	CLCC48	ceramics
BST1258-B	E (Military Temp Range)	QFN48	plastic