

BST08B64GA1

1. Product Overview

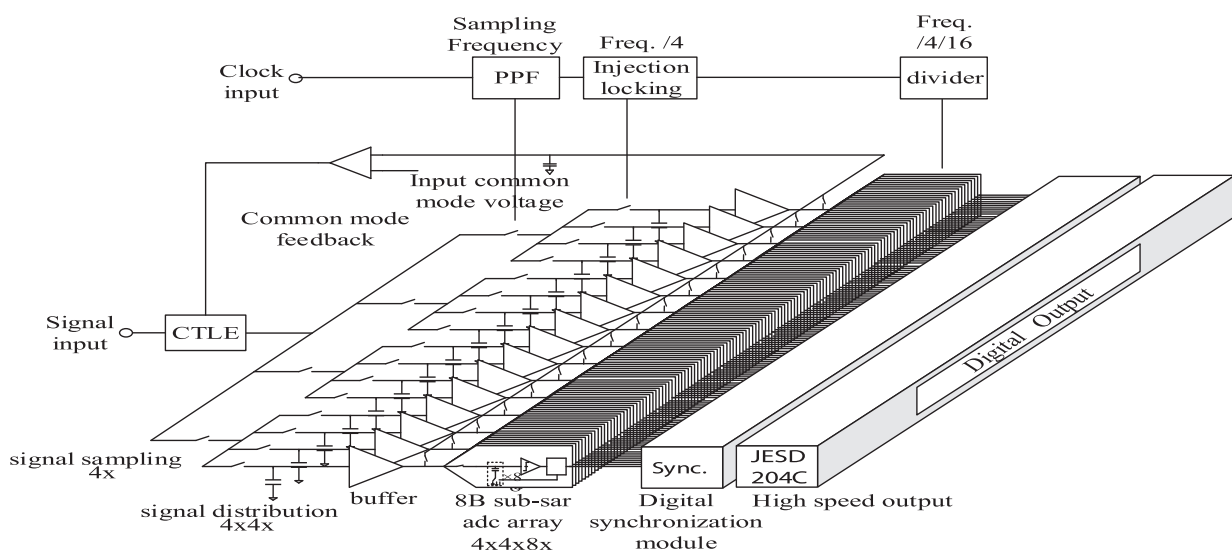
BST08B64GA1 is an 8-bit ultra-high-speed A/D converter with an adjustable sampling rate range of 32GSPS to 64GSPS and an input bandwidth of about 19GHz. The ADC core is implemented using a time-interleaved SAR structure. By using broadband sample-and-hold circuit design technology, time interleaving and internal error correction technology, and JESD204C high-speed serial interface circuit design technology, it has the ability of a single-chip high-speed and high-input bandwidth A/D converter, while having a low bit error rate (CER < 1e-14).

The BST08B64GA1 is available in a BGA484 package and is rated over the -40°C to +85°C industrial temperature range. The recommended ambient operating temperature is Below 50 degrees, thus ensuring the junction temperature inside the chip is less than 100 degrees, thereby obtaining better performance and stability.

2. Product Features

- NSD: -141.6 dBFS/Hz at 50 GSPS with -1dBFS, 1GHz input;
-142.0 dBFS/Hz at 50 GSPS with -3dBFS, 1GHz input.
- SFDR: 51.3 dBFS at 50 GSPS with -1dBFS, 1GHz input;
47.5 dBFS at 50 GSPS with -1dBFS, 10GHz input;
42.2 dBFS at 50 GSPS with -1dBFS, 20GHz input.
- Worst other spur (H2, H3 Except for : 5 1.3 dBFS at 50 GSPS with -1dBFS, 1GHz input.
- DNL Typical value ± 0.16 LSB; INL Typical value ± 0.46 LSB.
- Low bit error rate (CER) : $< 1 \times 10^{-14}$ (see Table 10 for test conditions).
- Low power consumption: typical value ≤ 4 W at 50 GSPS.
- Input bandwidth supports 19GHz About 500mVpp, 100Ω.
- Support SPI Interface, meet SPI Standard interface protocol, addressable internal storage space.
- 32 Lane JESD204C Output, maximum line rate up to 25Gbps, compatible with JESD204B interface.
- 19 × 19mm, 484-ball BGA package.

3. Functional Block Diagram



4. Electrical Parameters

4.1. Technical specifications

Unless otherwise specified, DVDD = DRVDD1 = 1.0V, AVDD = 1.1V, DRVDD2 = SVDDH = 2.5V, AIN = -1.0dBFS.

Table 1. Specifications

Parameter	Temperature	BST08B64GA1			Unit
		Minimum	Typical	Maximum	
Speed Grade		32	50	64	GSPS
Resolution		8			Bit
Accuracy					
No missing codes	Room temperature	ensure			
Offset error range	Room temperature	-3 ~ 3			LSB
Gain error range	Room temperature	-10 ~ 10			%FSR
Differential Nonlinearity (DNL)	Room temperature	±0.16			LSB
Integral Nonlinearity (INL)	Room temperature	±0.46			LSB
Analog Input					
Differential input voltage	Room temperature	450~580			mVpp
Differential input resistance	Room temperature	81			Ω
Input common mode voltage (Vcm)	Room temperature	0.5 ~ 0.9			V
Full power analog bandwidth	Room temperature	19			GHz
Input Referred Noise	Room temperature	0.8			LSB _{RMS}
Isolation					
Between analog power supply and digital power supply	Room temperature	FEXT, NEXT <- 50 dB(0~10GHz)			–
power supply					
D _{VDD}	Room temperature	0.975	1.0	1.025	V
A _{VDD}	Room temperature	1.080	1.1	1.120	V
D _{RVDD} ¹	Room temperature	0.975	1.0	1.025	V
D _{RVDD} ²	Room temperature	2.45	2.5	2.75	V
S _{VDDH}	Room temperature	1.8	2.5	2.75	V
I _{DVDD} ¹	Room temperature	0.6	A		
I _{AVDD} ¹	Room temperature	0.8	A		
I _{DRVDD1} ¹	Room temperature	0.9	A		
I _{DRVDD2} ¹	Room temperature	0.6	A		
I _{SVDDH} ¹	Room temperature	0.01	A		
Power _{consumption1}	Room temperature	4.0	W		

Note 1 : Note 1 in the table is the current and power consumption at 50G Sampling rate, 16-lane. The following test results.

4.1.1. Digital specifications

Unless otherwise specified, DVDD = DRVDD1 = 1.0V, AVDD = 1.1V, DRVDD2 = SVDDH = 2.5V, AIN = -1.0dBFS.

Table 2. Digital specifications

Parameter	Test conditions	Temperature	Typical Value	Unit
Clock Input				
Differential input voltage		Room temperature	1400	mVpp
Common mode input voltage		Room temperature	0.5	V
Input resistance (differential)		Room temperature	105	Ω
SYSREF enter (SYSREF_x)				
Differential input voltage		Room temperature	1000	mVpp
Common mode input voltage		Room temperature	0.85	V
Input resistance (differential)		Room temperature	103	Ω
Input Capacitance		Room temperature	0.5	pF
TRIG Input (TRIG_x)		Room temperature	1000	mVpp
Differential input voltage				
Common mode input voltage		Room temperature	0.85	V
Input resistance (differential)		Room temperature	105	Ω
Input Capacitance		Room temperature	0.5	pF
Logic input (MOSI, SCLK, CEB)				
Logic Compatibility		Room temperature	CMOS	
Voltage Logic 1		Room temperature	>0.7*SVDDH	V
Voltage logic 0		Room temperature	<0.3*SVDDH	V
Input resistance		Room temperature	44	kΩ
Input Capacitance		Room temperature	1.5	pF
SYNCINB_x enter				
Logic Compatibility		Room temperature	CML	
Voltage		Room temperature	1000	mV
Input resistance (differential)		Room temperature	32	kΩ
Input Capacitance		Room temperature	1	pF
Logic output (MISO)				
Logic Compatibility		Room temperature	CMOS	
Voltage Logic 1		Room temperature	>SVDDH - 0.45	V
Voltage logic 0		Room temperature	<0.45	V
Reset (RSTB)				
Voltage Logic 1		Room temperature	>0.7*SVDDH	V
Voltage logic 0		Room temperature	<0.3*SVDDH	V
Input resistance (differential)		Room temperature	44	kΩ
Input Capacitance		Room temperature	1.5	pF
REFCLK Input (REFCLK_x)				
Differential input voltage		Room temperature	1000	mVpp
Common mode input voltage		Room temperature	0.85	V
Input resistance (differential)		Room temperature	100	Ω
Input Capacitance		Room temperature	0.5	pF
EXT_CLK enter				
Input voltage		Room temperature	2.5	V
Input resistance		Room temperature	10	kΩ
Input Capacitance		Room temperature	0.5	pF

4.1.2. Switch Specifications

Unless otherwise specified, DVDD = DRVDD1 = 1.0V, AVDD = 1.1V, DRVDD2 = SVDDH = 2.5V, AIN = -1.0dBFS.

Table 3. Switch Specifications

Parameter	Test conditions	Temperature	Minimum	Typical	Maximum	Unit
Clock (CLK)						
Clock rate		Room temperature	8		16	GSPS
Clock Duty Cycle		Room temperature	45	50	55	% Duty Cycle
Uncertain (jitter)		Room temperature	50			(fs) rms
Latency						
Pipeline Delay		Room temperature	4672			Clock cycle
TRIG(TRIG_x)						
Build Time		Room temperature	1			ns
Keep Time		Room temperature	1			ns
Uncertain (jitter)		Room temperature	2			(ps) rms
Output Parameters (Serdout)						
Rise time		Room temperature	10			ps
Fall time		Room temperature	10			ps
Line Rate		Room temperature			25	Gbps

4.1.3. Timing Specifications

Table 4. Timing Specifications

Parameter	Test Conditions / Comments	Minimum	Typical Value	Maximum	Unit
SPI Timing requirements					
TdS	Data and SCLK Setup time between rising edges	8			ns
Td	Data and SCLK Hold time between rising edges	8			ns
Tclk	SCLK cycle	100			ns
Ts	CEB With SCLK The build time between	4			ns
Th	CEB With SCLK Keep time between	4			ns
Thigh	SCLK The minimum time that the	20			ns
Tlow	SCLK The minimum time that it should be in the logic low state	20			ns
Taccess	SCLK Between the falling edge and the read instruction outputting valid data Maximum delay time		12	20	ns

5. Ordering Information

Serial number	Model	Package	Packaging materials	Device level
1	BST08B64GA1PBGA484I	PBGA484	Plastic packaging	I class
2	BST08B64GA1PBGA484M3	PBGA484	Plastic packaging	N1 class
3	BST08B64GA1PBGA484E	PBGA484	Plastic packaging	Military Temperature

Note 1:

- a) I/ Industrial temperature range devices meet the screening requirements of Q/BST40022-2021 “General Specifications for Industrial Temperature Range Products of Huawei”, and their operating environment temperature range should be -40 ° C ~ +85 ° C.
- b) N/N1 grade devices meet GJB 7400 Screening requirements for level N/N1 of the General Specification for Semiconductor Integrated Circuits for Qualified Manufacturer Certification.
- c) Military temperature grade devices meet Q/BST40020-2018 According to the screening requirements of “General Specifications for HUAWEI Military-grade Products”, the operating environment temperature range should be -55 °C ~ +125 °C.

Note 2: The product ordering information is for our existing products or devices that have been confirmed to be developed. We can develop devices in other packaging forms according to user needs.