65W Series Radiation Hardened DC-DC Converter

Product Description

The 65W series radiation hardened DC-DC converter is a kind of hybrid integrated circuit, hermetically packaged by FPPa metal package. The input voltage range is from 80V~120V(typically is 100V) and the output power is 65W. The 65W series converters is capable of radiation hardness, SEE hardness to LET, and the device is featured with low output ripple voltage, stable output voltage and high quality grade etc.

Table 1. 65W series radiation hardened DC-DC converters

Model No.		Input voltage	Output current	Output voltage
BST/100-28-65/SP		80V～120V, typically 100V	0.232 A ~2.321A	Single 28V（±10% trimmable）

Product Features

- Operating temperature range (Tc) is from -55℃ to +125℃;
- Input DC voltage range is from 80V to 120V, typically 100V;
- Input, output and metal case are isolated from each other;
- Single ended topology and magnetic isolation are adopted in this circuit structure;
- Isolation capacitance is from 1000 pF/1000V to 3300 pF/1000V;
- Fixed switching frequency is from 260kHz to 360 kHz, and typically is 300kHz;
- The hybrid is capable of short circuit protection, disabling function (low level inhibiting) and under-voltage lockout protection (60V±5V);
- MTBF is more than 2×10^5h;
- Total dose is 100K rad(Si);

- SEE hardness to LET is up to 65MeV·cm2/mg;

Applications

Aerospace systems, communication systems, satellites, manned space engineering etc.

Operating conditions

Absolute maximum ratings

- Input voltage range is from 0V to 140V；
- Output power is 85 W；
- Operating temperature is from－55℃ to 125℃：
- Storage temperature is from－65℃ to 150℃；
- Lead temperature is 300℃ (10s)；

Notes：Device can not work with two or more maximum ratings at the same time.

Recommended operating conditions

- Input voltage is from 80V to 120V;
- Output power is from 13 to 65W（optimally is 20W, the recommended output power range is from 20% to 100%）;
- Operating temperature（TC）is from －55℃ to 125℃。

Marking and Designation

Device marking

Device marking includes the following items.:

- Device identification number;
- Lot identification code or date code;

- Manufacturer or trademark;
- Serial Number;
- ESDS identification code。

BST/100-28-65/SP M C R

| | | |

Device model Package type lead finish RHA grade

In addition, each device has a unique continuous number and shall be labled to identify the identification code of the sealing week. Equilateral triangle（Δ）serves as a mark of electrostatic sensitive devices, also used as the first pin.

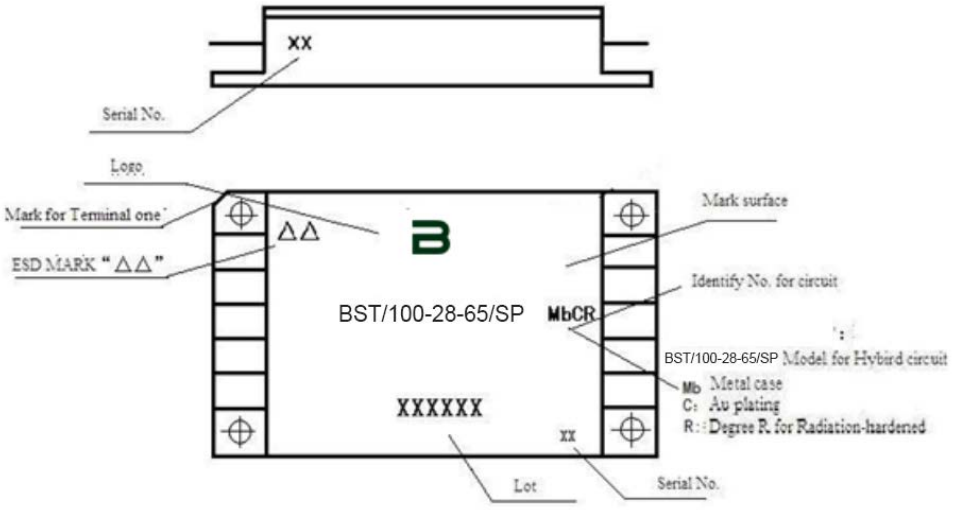


Fig.1. Diagram of the device marking

Device Designation

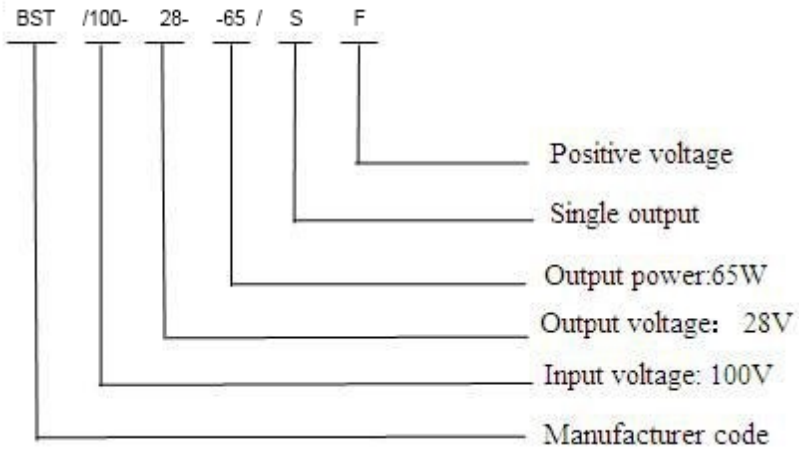
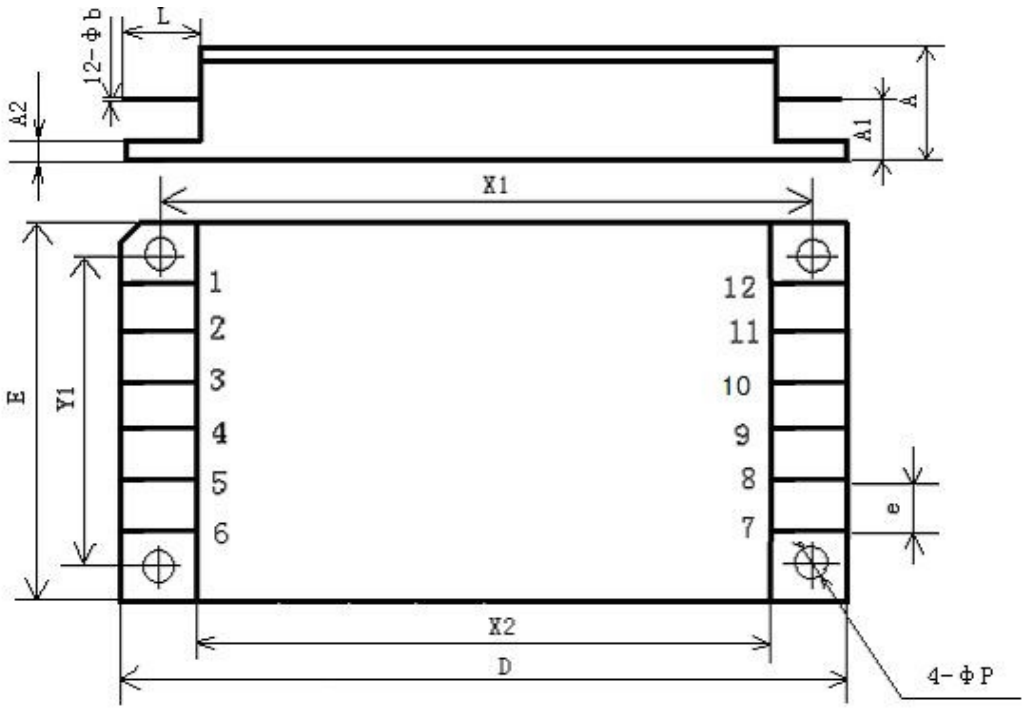


Fig.2. Diagram of the device designation

Mechanical outline



Unit: mm

Symbol		Data	
	Min	Typical	Max
A	-	-	10.66
A A1	-	5.59	-
A A2	-	1.27	-
B ϕb	-	1.00	-
D	-	-	76.70
A e	-	5.08	-
E	-	-	38.60
L	5.35	-	-
A ϕP	-	3.30	-
A X1	-	70.10	-
X2	-	-	64.00
A Y1	-	32.00	-
[a] Tolerance is ±0.30, [b] Tolerance is ±0.13.			

Fig.3. Mechanical specifications

Pin Designation

65W series device pin layout is shown in Fig. 4.

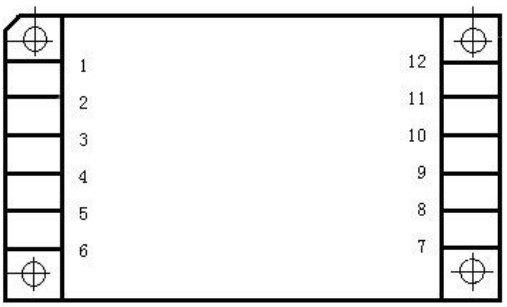


Fig.4. Pin layout diagram（top view）

Table.2. Pin layout arrangement

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	VIN	+ Input	7	V0	+ Output
2	GND_{IN}	Input Ground	8	GND_O	Output Ground
3	CASE	Case	9	NC	No Connection
4	INH	Inhibit	10	Trim	Output trimming
5	NC	No Connection	11	NC	No Connection
6	NC	No Connection	12	NC	No Connection

Electrical characteristics

Table 3. BST/100-28-65/SP electrical characteristics

No.	Features	Symbol	Conditions (-55℃≤T_C≤125℃, V_I =100V±0.5V, C_L=0, unless otherwise specified)	Group A Subgroup	Limits		Unit
					min	max	
1	Output current	VO	I_O=2.321A	1	27.72	28.28	V
				2，3	27.50	28.50	
2	Output voltage	IO	V_I=80V～120V	1,2,3	-	2321	mA
3	Output ripple(peak-	V_R	BW=20MHz， I_O=2.321A,	1	—	150	mV
	peak)		V_I=80V、100V、120V	2,3	—	200	
4	Line regulation	SV	V_I=80V→120V， I_O=2.321A	1,2,3	-	1	%
5	Load regulation	S_I	I_O=0→2.321A	1,2,3	—	1	%
6	Input current	IIN	I_{OUT}=100%, INH is connected with GNDin.	1,2,3	—	5	mA
			I_{OUT}=0%, INH opens.		—	50	

7	Input reflected ripple current (peak-peak)	IRIP	BW=20MHz, IO=2.321A, connected w ith EMI filter	1,2,3	—	80	mA
8	Input reflected rippl e voltage (peak-peak)	VRIP	BW=20MHz, IO=2.321A, connected w ith EMI filter	1,2,3	—	500	mV
9	Switching frequency [b]	fs	IO=2.321A	4,5,6	260	360	kHz
10	Efficiency	η	IO=2.321A	1	83	-	%
				2, 3	80	-	
11	Power dissipation, load fault	PD	Short circuit	1	-	25	W
12	Capacitance load [ab]	CL	No effect on DC performance	4	—	100	μF
13	Isolation	RISO	input to output or any pin to case except pin 3, test at 500V	1	100	—	MΩ
14	Vout response to load transition (peak)[bc]	VLOR	50% to/from 100% rated load, 10% to/from 50% rated load	4	-2240	2240	mV
15	Recovery time of Vout response to load transition[bcd]	tLOR	50% to/from 100% rated load, 10% to/from 50% rated load	4	—	5	ms
16	Vout responsetoVin transition(peak)[be]	VVOR	Input voltage VI：80→100V, 2.321A Input voltage VI：100→80V, 2.321A Input voltage VI：100→120V, =2.321A	4	-2800	2800	mV

			Input voltage V_I：120→100V, =2.321A IO = IO = IO IO				
17	Recovery time of Vout responsetoVin transition[bde]	tVOR	voltage V_I：80→100V, =2.321A voltage V_I：100→80V, =2.321A voltage V_I：100→120V, =2.321A voltage V_I：120→100V, =2.321A	4	—	5	ms
18	Start-up overshoot (peak)[b]	VTO	Input voltage V_I：0→100V, I_O= 2.321A	4,5,6	—	1680	mV
19	Start-up delay [f]	tTR	Input voltage VI：0→100V, IO =2.321A	4,5,6	—	100	ms
20	Load failure recovery time[bd]	tLF	I_O from short circuit to 2.321A	4	—	10	ms
21	Inhibit input	VINH		1	—	15	V
22	Protection power	PW		1	85	—	W

- Capacitive load may be any value from 0 to the maximum limit, without compromising dc parameter.
- The parameter is guaranteed by design, and tested only when there is inspection and change in design or process.
- Load transition time shall be from 10μs to 15μs.
- Recovery time is from the initiation of the transition to the time Vout has returned to steady value within ±1% .
- Line transient time shall be more than 50μs.
- Start-up delay can be calculated from either the initiation of the converter transition or the removal of the grounded inhibit pin.

Application Notes

Electrical connection

Test connection is shown in Fig. 5.

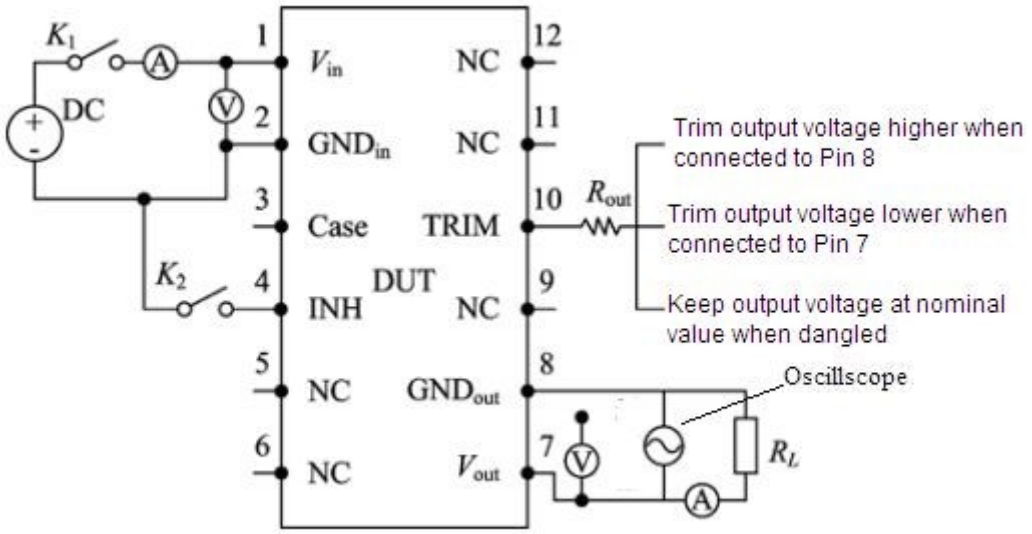


Fig.5. Product electrical connection diagram

Inhibit function

The device has inhibit function, inhibiting at low voltage (<0.2V). The device operates normally at high voltage (13V~25V) or when dangled. When the device is inhibited, input current shall be less than 2mA and output voltage shall be less than 0.5V.

The device does not output, when the inhibit pin (INH) is grounded directly, or connected with external NPN transistor (set base high level), as shown in Fig. 6. When the inhibit pin is dangled, the voltage is 8.5V-13V DC. Both resistance and capacitance in the Fig. 6 can be appropriately adjusted. The inhibit pin can be dangled when it is not needed.

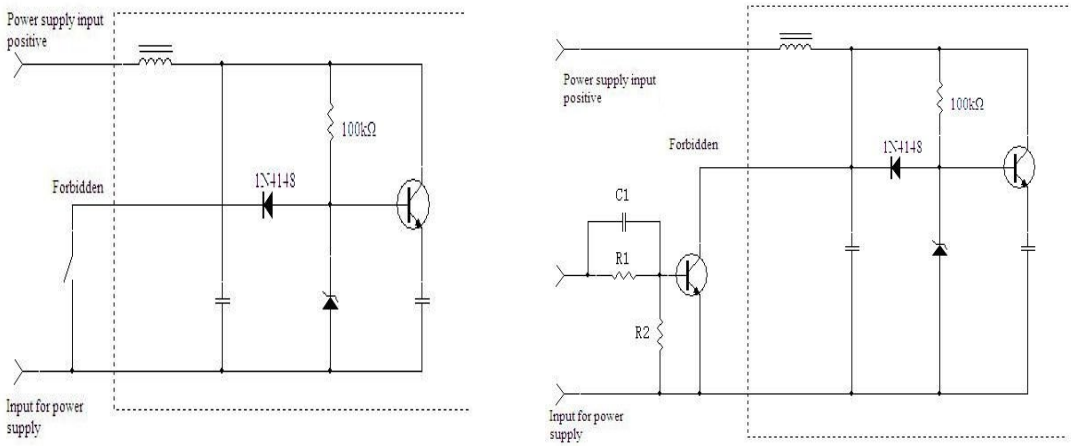


Fig.6. Inhibit pin connection Diagram

Short circuit protection function

The series device has short circuit protection function. When output pin shorts, the device is turned into protection state (belching like protection, squeaking sound). Here, output voltage is close to 0V, bus-line current is about 120mA to 250mA, internal power dissipation inside is about 12W to 25W when shorts. The parameters above are tested at the bottom of output pin at the normal temperature.

Under-voltage protection function

This series product have under voltage protection function, when input voltage is below 60V±5V, the product does not have output voltage.

Surge protection capability

Surge protection voltage of the series device is 160V/1ms. It is recommended for user to consider input port high voltage.

Design of surge protection circuit at front end

LC filter circuit is used at input port inside of the device. At the moment of power start-up, there is inevitably high surge current because ESR of capacitor is small (mΩ level). So it is recommended for user to add surge protection circuit or select EMI filter with surge protection circuit.

Surge protection circuit is shown in Fig. 7:

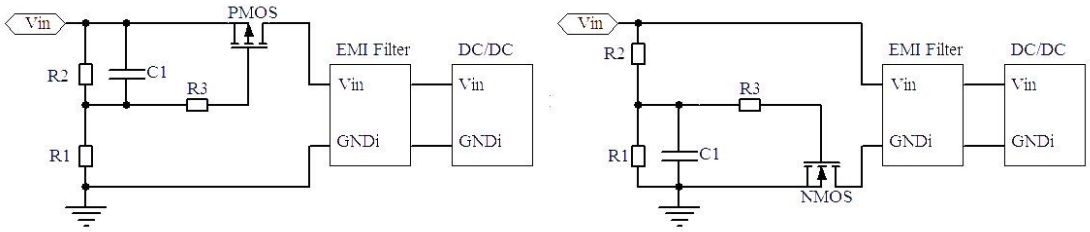


Figure 7. Surge protection circuit

It is recommended to use R1=95kΩ, R2=10kΩ, R3=20Ω, C1=1μF. Charge and discharge time can be controlled by changing the value of C1. The withstand voltage of P channel and N channel MOSFET should be more than 200V. Current should be considered according to the bus bar current, coupled with grade 1 derating design. It is recommended that input voltage rise time of DC/DC converter shall be more than 1ms. C1 capacitance shall be set by the user according to the actual system application.

Design of output filter at back-end

LC filter circuit is used internally. If output ripple can not meet the requirements of the system, filter circuit can be redesigned at the output port of DC/DC converter in order to reduce the ripple. Several recommended filter circuits are as follows.:

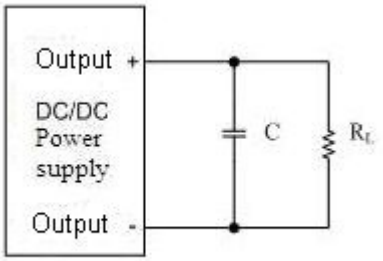


Fig.8 Connected with capacitor

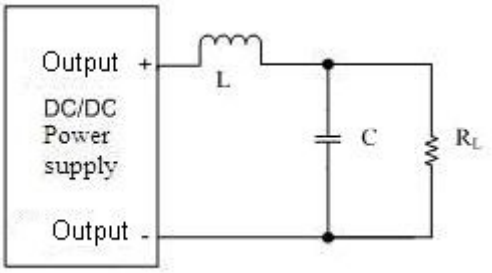


Fig.9 Connected with LC filter

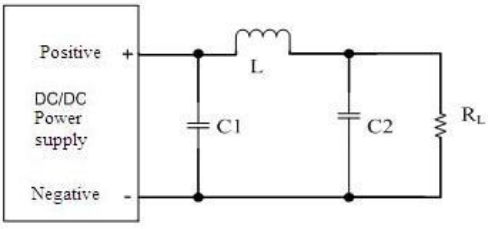
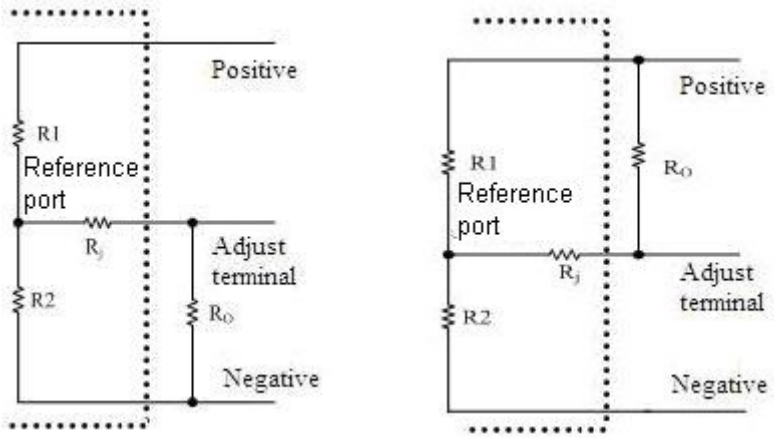


Fig.10. Connected with Π type filter

Capacitor shall be mounted as close to the load side as possible, and capacitance of the external capacitor shall be less than the capability of the converter with capacitive load; The inductance of inductor L can be adjusted according to the actual application.

Use of single output adjustment end



(a) Output voltage up (b) Output voltage down

Fig.11. Adjustment end of single output connection figure

As shown in Fig. 11, R1, R2, Rj are internal resistors of the converter, and Ro is an external resistor, fine-trimming output voltage of DC/DC converter. Firstly, potentiometer is used to debug output voltage, and then replaced with precision resistor. The power of resistor shall be no less than 1/10W.

Table 4.Selection of resistors at adjustment end of BST/100-28-65/SP

BST/100-28-65/SP Output voltage up V_{OH}						BST/100-28-65/SP Output voltage down V_{OL}					
R1	R2	Vref	Rj	R_O	VOH	R1	R2	Vref	Rj	R_O	VOL
（K）	（K）	（V）	（K）	（**K**）	（V）	（K）	（K）	（V）	（K）	(K)	（V）
53	3	1.5	26.5	260	28.28	53	3	1.5	26.5	5000	27.72
				116	28.56					2450	27.44
				68	28.84					1600	27.16
				44.5	29.12					1170	26.88

				30.3	29.40					925	26.60
				20.8	29.68					759	26.32
				14	29.96					638	26.04
				9	30.24					548	25.76
				5	30.52					478	25.48
				1.9	30.80					422	25.20

Typical output waveform

Start-up delay/start-up overshoot（T_C=25℃, V_{in}=100V±0.5V, full load）

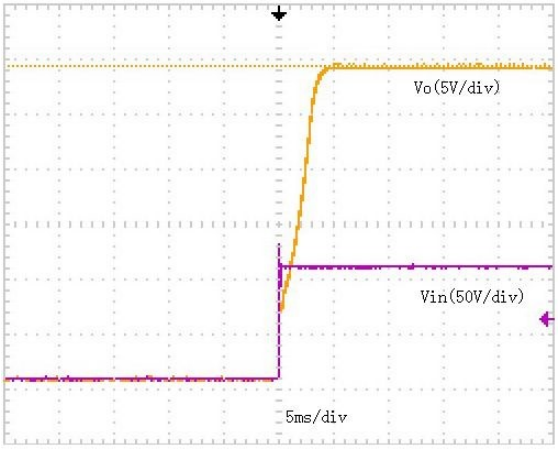


Fig.12. BST/100-28-65/SP Start-up delay/start-up overshoot

4.2 Load step curve（T_C=25℃，V_{in}=100V±0.5V）

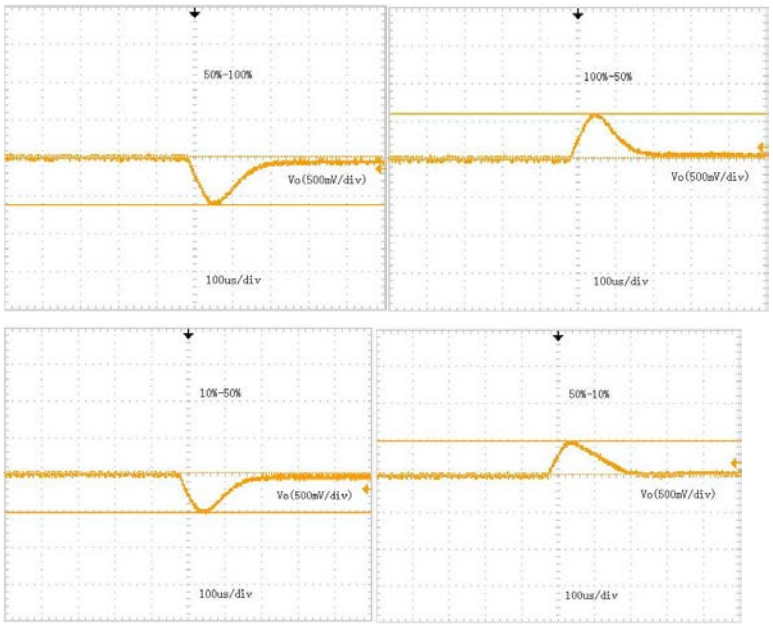


Fig. 13. BST/100-28-65/SP Load step curve

4.3 Line step curve（T_C=25℃，full load）

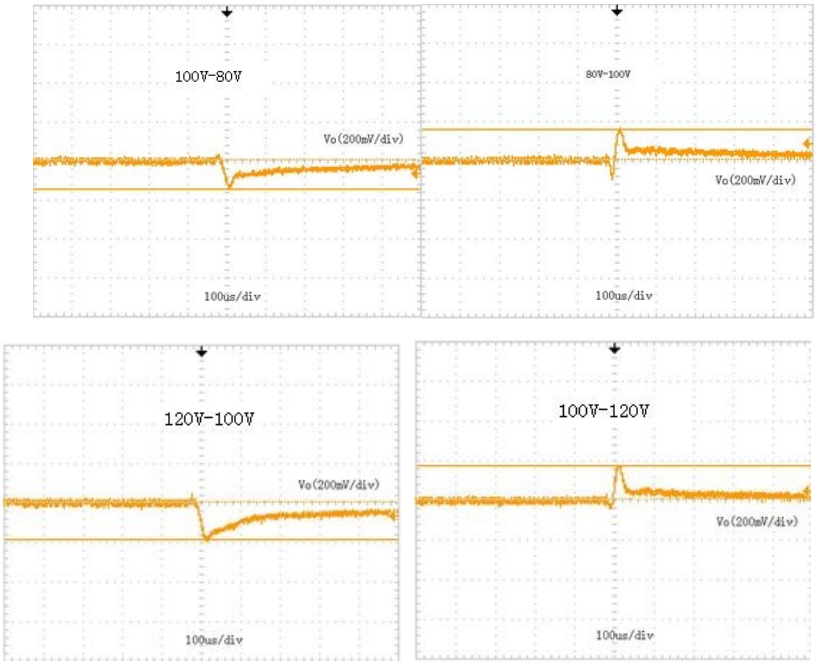


Fig.14. Line step BST/100-28-65/SP

Output efficiency curve

Output power-efficiency curve（T_C=25℃，V_{in}=100V±0.5V）

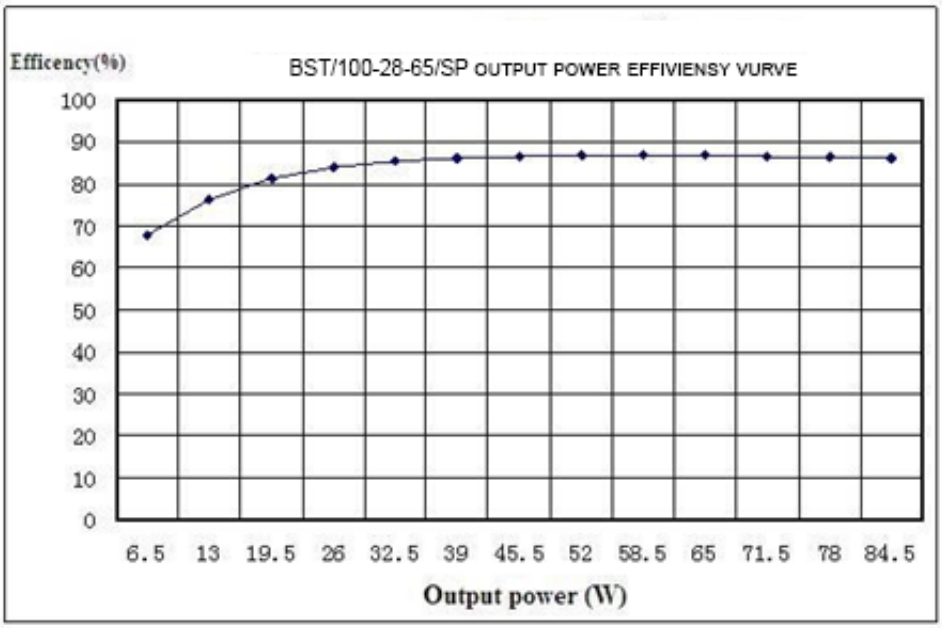


Fig.15. Output power-efficiency curve of BST/100-28-65/SP

5.2 Input voltage- efficiency curve（T_C=25℃，full load）

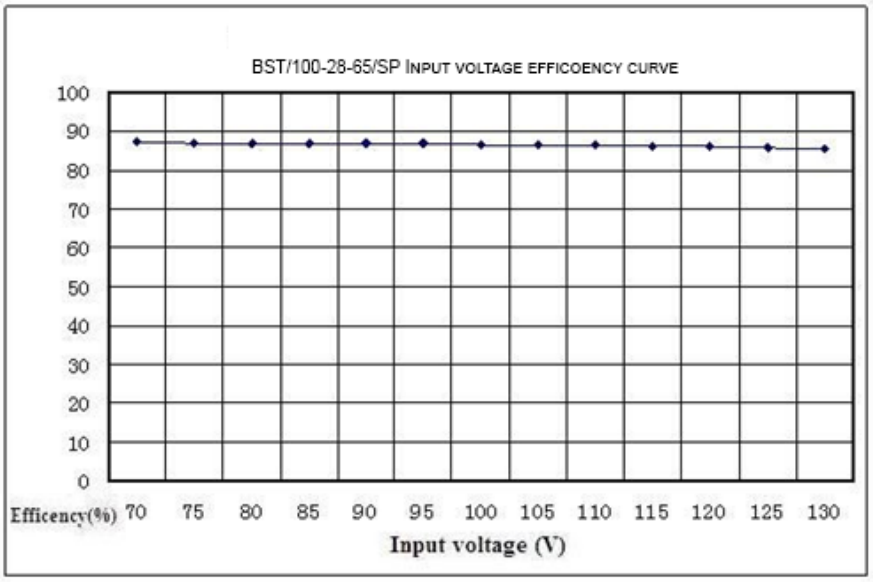
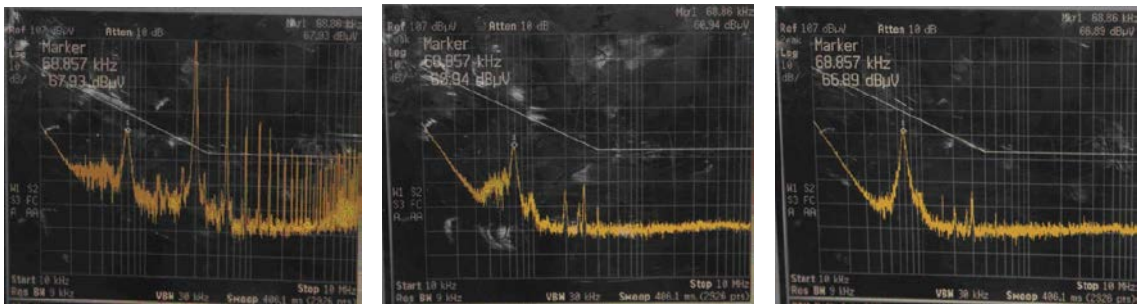


Fig.16. Input voltage- efficiency curve of BST/100-28-65/SP

Effect of CE102 after using EMI filter



Without filter With BST100-461-80 filter With BST100-461-300 filter

Fig.17. BST/100-28-65/SP

MTBF curve

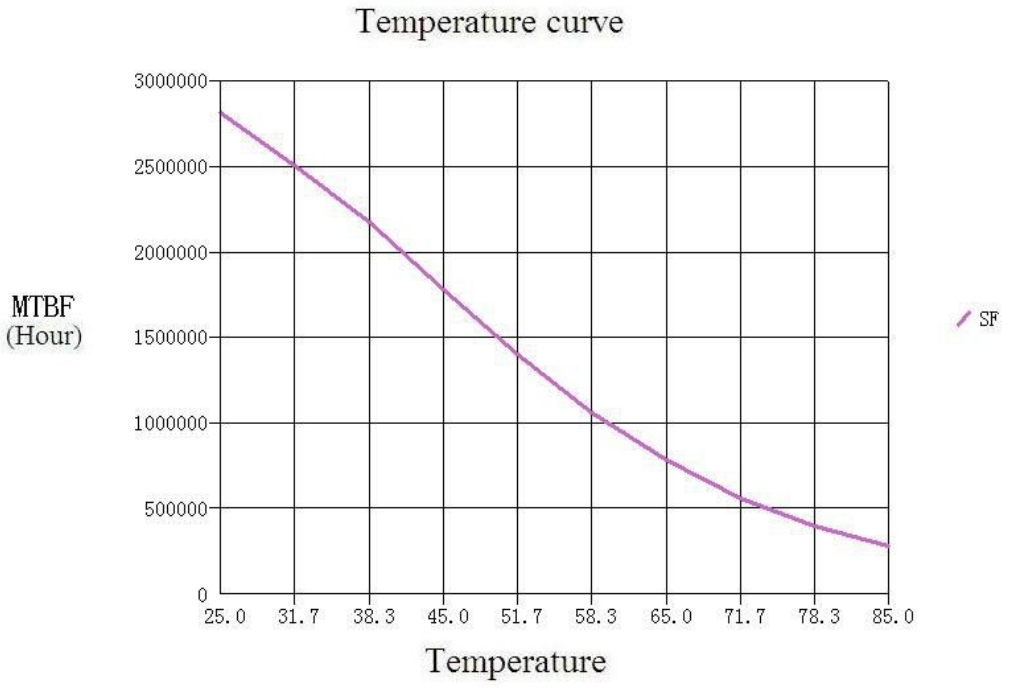


Fig.18. BST/100-28-65/SP

Internal thermal resistance

Metal case of this series of devices are made of cold rolled steel which has higher thermal conductivity. Internal thermal resistance is shown in Table 5.

Table 5. Internal thermal resistance

Model	Internal thermal resistance（℃/W)	Heat sink dimensions (mm^3)	Power (w)	Heat sink material
BST/100-28-65/SP	2.4	300×200×2 mm^3	11.47	Copper

Attention

- Case pins shall not be bent to avoid bruising insulators to affect device hermeticity.
- Check the polarity of input power line before powering on so as to avoid permanent failure caused by powering on suddenly.
- Check load conditions carefully during operation to avoid instability.
- Take electrostatic protection measures during storing, transporting, installing and debugging.
- Observe “User Manual” during storing, operation and soldering.
- Keep away from high voltage input terminal during operation.
- Heat sink shall be used with the device to keep the case temperature below 125 ºC.
- The bus voltage rise time shall be more than 1ms.