5W Series Radiation Hardness DC-DC Converter

Product Overview

The 5W series radiation hardness DC-DC converter is a kind of hybrid integrated circuit, hermetically packaged by UPPa metal package. The input voltage range is from 80V to 120V, typically is 100V while output power is 5W. The 5W series converter is capable of radiation hardness, SEE hardness to LET, and the device is featured with low output ripple voltage, stable output voltage and high quality grade etc.

Table 1 5W series radiation hardened DC-DC converters

Model No.	Input voltage	Output current	Output voltage
BST/100-5-5/SP	80V～120V，typically 100V	0.1 A ~1A	Single 5V（±10％ trimmable）
BST/100-15-5/SP	80V～120V，typically 100V	0.033 A ~0.333A	Single 15V（±10％ trimmable）
BST/100-3R3-5/SP	80V～120V，typically 100V	0.152A~1.515A	Single 3.3V（±10％ trimmable）
BST/100-5-5/D1	80V～120V，typically 100V	0.05A~0.5A	Dual ±5V
BST/100-12-5/D1	80V～120V，typically 100V	0.021A~0.208A	Dual ±12V

Product Features

- Operating temperature range (Tc) is from -55℃ to +125℃.
- Input DC voltage range is from 80V to 120V, and typically is 100V.
- Input, output and metal case are isolated from each other.
- Single ended topology and magnetic isolation are adopted in this circuit structure.
- Isolation capacitance is from 1000 pF/1000V to 3300 pF/1000V.
- Fixed switching frequency is from 260kHz to 360 kHz, typically 300kHz.
- The device is capable of short circuit protection, disabling function (low level inhibiting) and under-voltage lockout protection (60V±5V).

- MTBF is more than 2×105h.
- Total dose is 100K rad(Si).
- SEE hardness to LET is up to 65MeV·cm2/mg
- Weight：32g～38g； Dimension：37.33mm×28.94 mm×8.90 mm；

Applications

Aerospace systems, communication systems, satellites, manned space engineering etc.

Operating conditions

- Absolute maximum ratings
- Input voltage range is from 0V to 140V.
- Output power is 6.5W.
- Operating temperature is from -55℃ to 125℃.
- Storage temperature is from -65℃ to 150℃.
- Lead temperature is 300℃ (10s).

Notes: Device can not work with two or more maximum ratings at the same time.

Recommended operating conditions

- Input voltage is from 80V to 120V.
- Output power is from 1W to 5W（ optimally 5W, the recommended output power range is from 20% to 100%.）
- Case operating temperature (TC) is from -55℃ to 125℃.

Device Marking and Designation

Device marking

- Device marking is defined in detail specification, including the following items.
- Device identification number
- Orientation point
- Lot identification code or date code
- Manufacturer or trademark
- Serial Number
- ESDS identification code

BST/100-5-5/SP M C R

Device model Package type lead finish RHA grade

In addition, each device has a unique continuous number and should be labeled to identify the identification code of the sealing week. Equilateral triangle（Δ）serves as a mark of electrostatic sensitive devices, also used as the first pin.

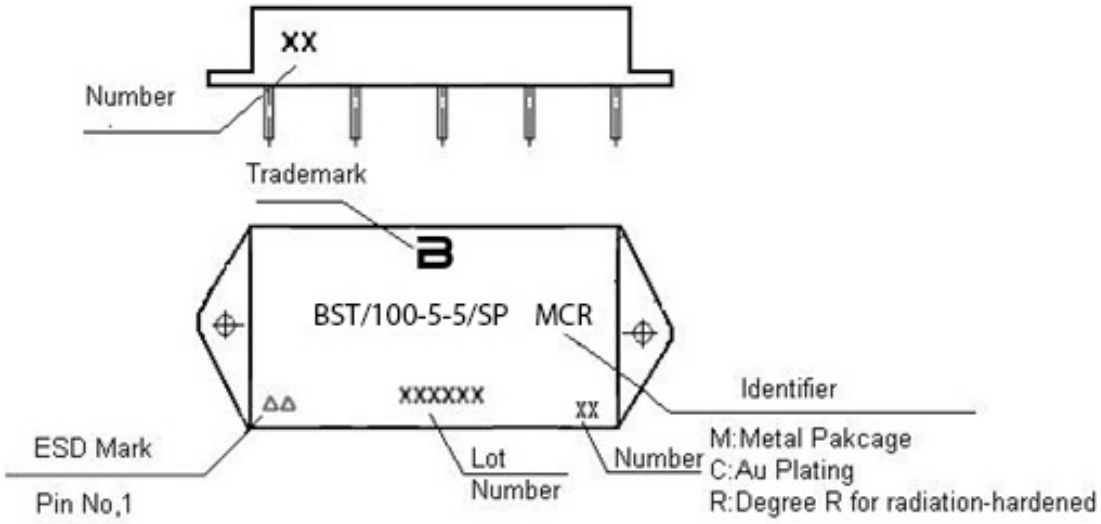


Fig. 1 Diagram of the device marking

Device Designation

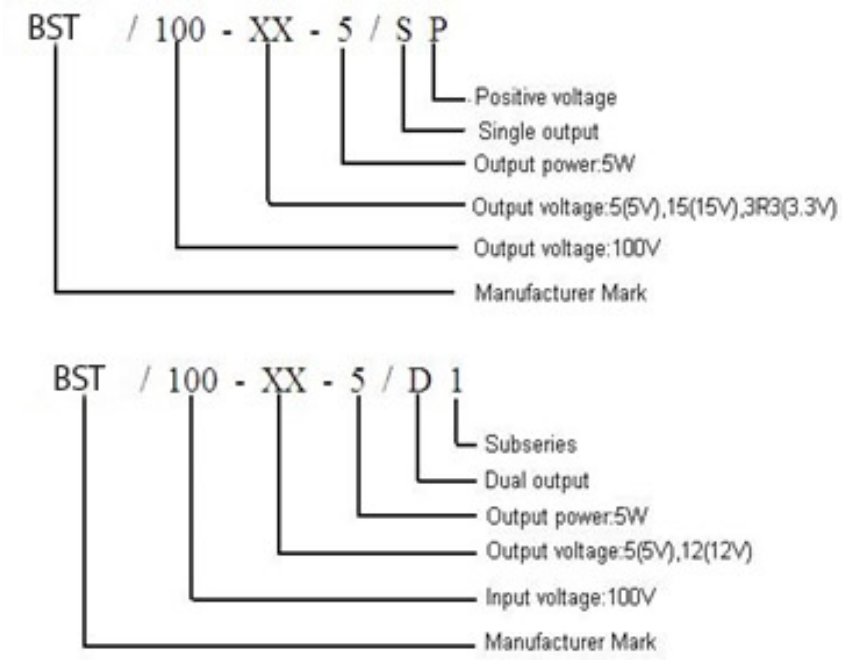


Fig. 2 Diagram of the device designation

Mechanical Specifications

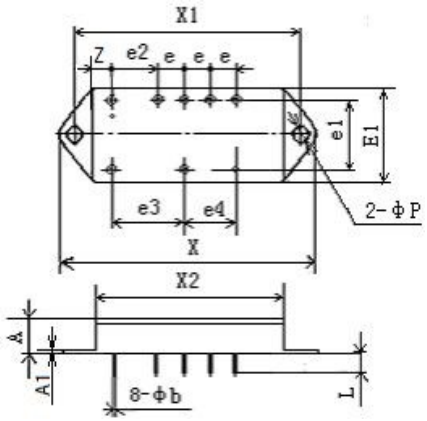


Fig. 3 UPPa mechanical specifications

Symbol	Data		
	Min	Typical	Max
A	-	-	8.90
A1 a	-	1.50	-
фb b	-	0.76	-
e a	-	5．08	-
e1 a	-	20．32	-
e2 a	-	7．62	-
e3 a	-	12．70	-
e4 a	-	10．16	-
E1	-	-	28.94
L	5.35	-	-
Φp a	-	3.30	-
X	-	-	51.30
X1 a	-	43.95	-
X2	-	-	37.33
Z	4.91	-	5.51
a Tolerance is ±0.30； b Tolerance is ±0.13。			

Unit: mm

1.6 Pin Designation

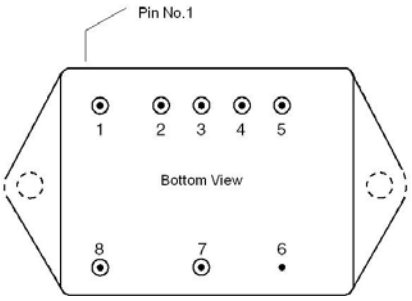


Fig. 3 Pin layout diagram (top view） Table.1 Pin layout arrangement（Single）

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	INH	Inhibit	5	Trim	Voltage Trimming
2	NC	No Connect	6	GND_C	Case Ground
3	GND_O	Output Ground	7	GND_{IN}	Input Ground
4	V_O	+ Output	8	V_{IN}	+ Input

Table.4 Pin layout arrangement（Dual）

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	INH	Inhibit	5	NC	No Connect
2	VO+	+ Output	6	GNDC	Case Ground
3	GNDO	Output Ground	7	GNDIN	Input Ground
4	VO-	- Output	8	VIN	+ Input

Electrical characteristics

Table 5 Electrical specifications of BST/100-5-5/SP

No.	Features	Symbol	Conditions(-55℃≤TC≤125℃，VI＝100V±0.5V, CL=0, unless otherwise specified)	Group A Subgroup	Limits Min	Limits Min	Units
1	Output voltage	VO	IO=1A	1	4.95	5.05	V
				2，3	4.85	5.15	
2	Output current	IO	VI=80V～120V	1,2,3	-	1000	mA
3	Output ripple(peak-peak)	VR	BW=20MHz，IO=1A，	1	—	80	mV
			VI=80V、100V、120V	2,3	—	120	
4	Line regulation	SV	VI=80V→120V，IO=1A	1,2,3	-	1	%
5	Load regulation	SI	IO=0→1A	1,2,3	—	1	%
6	Input current	IIN	IOUT=100%, INH is connected with GNDin.	1,2,3	—	5	mA
			IOUT=0%, INH opens.		—	50	
7	Input reflected ripple current(peak-peak)	IRIP	BW=20MHz，IO=1A，connected with EMI filter	1,2,3	—	80	mA
8	Input reflected ripple voltage(peak-peak)	VRIP	BW=20MHz，IO=1A，connected with EMI filter	1,2,3	—	100	mV
9	Switching frequency b	fs	IO=1A	4,5,6	260	360	kHz
10	Efficiency	η	IO=1A	1	68	-	%
				2,3	65	-	

11	Power dissipation	PD	Short circuit	1	-	4	W
12	Capacitance load[ab]	CL	No effect on DC performance	4	—	330	μF
13	Isolation	RISO	input to output or any pin to case except pin 6, test @ 500V	1	100	—	MΩ
14	Vout response to load transition(peak)[bc]	VLOR	Half load to/from full load	4	-400	400	mV
15	Recovery time of Vout response to load transition[bcd]	t_{LOR}	Half load to/from full load	4	—	5	ms
16	Vout response to Vin transition(peak)[be]	VVOR	Input voltage VI：80→100V, IO =1A Input voltage VI：100→80V, IO =1A Input voltage VI：100→120V, IO =1A Input voltage VI：120→100V, IO =1A	4	-500	500	mV
17	Recovery time of Vout response to Vin transition[bde]		Input voltage VI：80→100V, IO =1A Input voltage VI：100→80V, IO =1A Input voltage VI：100→120V, IO =1A Input voltage VI：120→100V, IO =1A	4	—	5	ms

		^{t}VOR					
18	Start-up overshoot(peak)b	VTO	Input voltage :VI：0→100V, IO =1A	4,5,6	—	300	mV
19	Start-up delay[f]	^{t}TR	Input voltage VI：0→100V, IO =1A	4,5,6	—	100	ms
20	Load failure recovery time[bd]	^{t}LF	IO=short current to 1A	4	—	10	ms
21	Inhibit input	VINH		1	—	15	V
22	Protection power	PW		1	6.5	—	W

a Capacitive load may be any value from 0 to the maximum limit, without compromising dc parameter.

b The parameter is guaranteed by design, and tested only when there is inspection and change in design or process.

c Load transition time shall be from 10μs to 15μs.

d Recovery time is from the initiation of the transition to the time Vout has returned to steady value within ±1% .

e Line transient time shall be more than 50μs.

f Start-up delay can be calculated from either the initiation of the converter transition or the removal of the grounded inhibit pin.

Table 6 Electrical Characteristics of BST/100-15-5/SP

No.	Features	Symbol	Conditions(-55℃≤TC≤125℃，VI＝100V±0.5V, CL=0, unless otherwise specified)	Group A Subgroup	Limits		Units.
					Min	Max	
1	Output voltage	VO	IO=0.333A	1	14.85	15.15	V
				2,3	14.70	15.30	
2	Output current	IO	VI=80V～120V	1,2,3	-	333	mA
3	Output ripple(peak-peak)	VR	BW=20MHz，IO=0.333A，VI=80V、100V、120V	1	—	100	mV
				2,3	—	150	
4	Line regulation	SV	VI=80V→120V，IO=0.333A	1,2,3	-	1	%
5	Load regulation	SI	IO=0→0.333A	1,2,3	—	1	%
6	Input current	IIN	IOUT=100%, INH is connected with GNDin.	1,2,3	—	5	mA
			IOUT=0%, INH opens.		—	50	
7	Input reflected ripple current(peak-peak)	IRIP	BW=20MHz，IO=0.333A，connected to EMI filter	1,2,3	—	80	mA
8	Input reflected ripple voltage(peak-peak)	VRIP	BW=20MHz，IO=0.333A，connected to EMI filter	1,2,3	—	100	mV
9	Switching frequency		IO=0.333A	4,5,6	260	360	kHz

	b	fs					
10	Efficiency	η	IO=0.333A	1 2,3	68 65	- -	%
11	Power dissipation	PD	Short	1	-	4	W
12	Capacitance load[ab]	CL	No effect on DC performance	4	—	100	μF
13	Isolation	RISO	Input to output or any pin to case except pin 6, test at 500V	1	100	—	MΩ
14	Vout response to load transition(peak)[bc]	VLOR	Half load to/from full load	4	-1200	1200	mV
15	Recovery time of Vout response to load transitionb[cd]	t_{LOR}	Half load to/from full load	4	—	5	ms
16	Vout response to Vin transition(peak)[be]	VVOR	Input voltage VI：80→100V, IO =0.333A Input voltage VI：100→80V, IO =0.333A Input voltage VI：100→120V, IO =0.333A Input voltage VI：120→100V, IO =0.333A	4	-1500	1500	mV

17	Recovery time of Voutresponseto Vin transition[bde]	t_{VOR}	Input voltage VI：80→100V, IO =0.333A Input voltage VI：100→80V, IO =0.333A Input voltage VI：100→120V, IO =0.333A Input voltage VI：120→100V, IO =0.333A	4	—	5	ms
18	Start-up overshoot(peak)[b]	VTO	Input voltage :VI：0→100V, IO =1A	4,5,6	—	900	mV
19	Start-up delayf	t_{TR}	Input voltage VI：0→100V, IO =1A	4,5,6	—	100	ms
20	Load failure recovery time[bd]	t_{LF}	IO=short current to 1A	4	—	10	ms
21	Inhibit input	VINH		1	—	15	V
22	Protection power	PW		1	6.5	—	W

a Capacitive load may be any value from 0 to the maximum limit, without compromising dc parameter.

b The parameter is guaranteed by design, and tested only when there is inspection and change in design or process.

c Load transition time shall be from 10μs to 15μs.

d Recovery time is from the initiation of the transition to when Vout has returned to steady value within ±1% .

e Line transient time should be more than 50μs.

f Start-up delay can be calculated from either the initiation of the converter transition or the removal of the grounded inhibit pin.

Table 7 Electrical Characteristics of BST/100-3R3-5/SP

No.	Features	Symbol	Conditions(-55℃≤TC≤125℃，VI＝100V±0.5V, CL=0, unless otherwise specified)	Group A Subgroup	Limits		Units
					Min	Max	
1	Output voltage	VO	IO=1.515A	1	3.267	3.333	V
				2，3	3.15	3.45	
2	Output current	IO	VI=80V～120V	1,2,3	-	1515	mA
3	Output ripple(peak-peak)	VR	BW=20MHz，IO=1.515A， VI=80V、100V、120V	1	—	80	mV
				2,3	—	120	
4	Line regulation	SV	VI=80V→120V，IO=1.515A	1,2,3	-	1	%
5	Load regulation	SI	IO=0→1.515A	1,2,3	—	2	%
6	Input current	IIN	IOUT=100%, INH is connected with GNDin.	1,2,3	—	5	mA
			IOUT=0%, INH opens.		—	50	
7	Input reflected ripple current(peak-peak)	IRIP	BW=20MHz，IO=1.515A，connected to EMI filter	1,2,3	—	80	mA
8	Input reflected ripple voltage(peak-peak)	VRIP	BW=20MHz，IO=1.515A，connected to EMI filter	1,2,3	—	100	mV
9	Switching frequency b	fs	IO=1.515A	4,5,6	260	360	kHz
10	Efficiency	η	IO=1.515A	1	60	-	%
				2,3	57	-	

11	Power dissipation	PD	short circuit	1	-	4	W
12	Capacitance load[ab]	CL	No effect on dc performance	4	—	330	μF
13	Isolation	RISO	Input to output or any pin to case (except pin 6) at 500V	1	100	—	MΩ
14	Vout response to load transition(peak)[bc]	VLOR	50% to/from 100% rated load, 10% to/from 50% rated load	4	-260	260	mV
15	Recovery time of Vout response to load transition[bcd]	tLOR	50% to/from 100% rated load, 10% to/from 50% rated load	4	—	5	ms
16	Voutresponse to Vin transition(peak)[be]	VVOR	Input voltage VI：80→100V, IO =1.515A Input voltage VI：100→80V, IO =1.515A Input voltage VI：100→120V, IO =1.515A Input voltage VI：120→100V, IO =1.515A	4	-330	330	mV
17	Recovery time of Voutresponse to Vin transition[bde]	tVOR	Input voltage VI：80→100V, IO =1.515A Input voltage VI：100→80V, IO =1.515A Input voltage VI：100→120V, IO =1.515A Input voltage VI：120→100V, IO =1.515A	4	—	5	ms

18	Start-up overshoot(peak)b	VTO	Input voltage VI：0→100V, IO =1.515A	4,5,6	—	200	mV
19	Start-up delayf	tTR	Input voltage VI：0→100V, IO =1.515A	4,5,6	—	100	ms
20	Load failure recovery timebd	tLF	IO from short circuit to 1.515A	4	—	10	ms
21	Inhibit input	VINH		1	—	15	V
22	Protection power	PW		1	6.5	—	W

a Capacitive load may be any value from 0 to the maximum limit, without compromising dc parameter.

b The parameter is guaranteed by design, and tested only when there is inspection and change in design or process.

c Load transition time shall be from 10μs to 15μs.

d Recovery time is from the initiation of the transition to when Vout has returned to steady value within ±1% .

e Line transient time should be more than 50μs.

f Start-up delay can be calculated from either the initiation of the converter transition or the removal of the grounded inhibit pin.

Table 8 Electrical Characteristics of BST/100-12-5/D1

No.	Features	Symbol	Conditions(-55℃≤TC≤125℃，VI＝100V±0.5V, CL=0, unless otherwise specified)	Group A Subgroup	Limits		Units
					Min	Max	
		VO1		1	11.88	12.12	
				2,3	11.64	12.36	
				1	-12.12	-11.88	

1	Output voltage	VO2	IO1=IO2=0.208A	2,3	-12.36	-11.64	V
2	Output Current	IO1	VI=80V～120V	1,2,3	-	208	mA
		IO2			-	208	
3	Output ripple voltage	VR1	BW=20MHz，IO1=IO2=0.208A，	1	—	100	mV
	(peak-peak)		VI=80V、100V、120V	2,3	—	150	
		VR2		1	-	100	
				2,3	-	150	
4	Voltage regulation rate	SV1	VI=80V→120V，IO1=IO2=0.208A	1,2,3	-	1	%
		SV2			-	1	
5	Load regulation rate	SI1	IO1=IO2=0→0.208A	1,2,3	—	1	%
		SI2			—	1	
6	Input Current	IIN	IOUT=100%, INH is connected with GNDin.	1,2,3	—	5	mA
			IOUT=0%, INH opens.		—	50	
7	Input ripple current (peak-peak)	IRIP	BW=20MHz，IO1=IO2=0.208A，connected to EMI filter	1,2,3	—	80	mA
8	Input ripple voltage （p-p）	VRIP	BW=20MHz，IO1=IO2=0.208A，connected to EMI filter	1,2,3	—	100	mV
9	Switching	fs	IO1=IO2=0.208A	4,5,6	260	360	kHz

	frequency b						
10	Efficiency	η	IO1=IO2=0.208A	1	68	—	%
				2,3	65	—	
11	Power dissipation short circuit	PD	Both output short circuit	1	—	4	W
12	Capacitive loadab	CL1	No effect on dc performance	4	—	100	μF
		CL2			—	100	
13	Isolation	RISO	Input to output or any pin to case (except pin 6) at 500V	1	100	—	MΩ
14	Vout response to load transition(peak)bc	VLOR1	50% to/from 100% rated load, 10% to/from 50% rated load Each output with balanced load.	4	-960	960	mV
		VLOR2			-960	960	
15	Recovery time of V out response to load transitionbcd	tLOR	50% to/from 100% rated load, 10% to/from 50% rated load Each output with balanced load.	4	—	5	ms
16	Vout response to Vin transition(peak)be	VVOR1	Input voltage VI:80→100V, IO1=IO2 =0.208A Input voltage VI：100→80V, IO1=IO2	4	-1200	1200	mV
		VVOR2			-1200	1200	

			=0.208A				
			Input voltage VI：100→120V, IO1=IO2 =0.208A Input voltage VI：120→100V, IO1=IO2 =0.208A				
17	Recovery time of Vout responseto Vin transitionbde		Input voltage VI:80→100V, IO1=IO2 =0.208A Input voltage VI：100→80V, IO1=IO2 =0.208A Input voltage VI：100→120V, IO1=IO2 =0.208A Input voltage VI：120→100V,	4	—	5	ms

		tVOR	IO1=IO2 =0.208A				
18	Start-up overshoot(peak)b	VTO1 VTO2	Input voltage VI:=0V→100V, IO1=IO2=0.208A	4,5,6	— −720	720 —	mV
19	Start-up overshoot(peak)b	tTR	Input voltage VI：0→100V, IO1=IO2=0.208A	4,5,6	—	100	ms
20	Load failure recovery timebd	tLF	IO1、IO2 from short circuit to 0.208A	4	—	10	ms
21	Inhibit input	VINH		1	—	15	V
22	Protection power	PW		1	6.5	—	W
23	Cross regulation	SC	One output with 50% load，the other output with 50% ~100% rated load	1,2,3	—	6	%

a Capacitive load may be any value from 0 to the maximum limit, without compromising dc parameter.

b The parameter is guaranteed by design, and tested only when there is inspection and change in design or process.

c Load transition time shall be from 10μs to 15μs.

d Recovery time is from the initiation of the transition to the time Vout has returned to steady value within ±1% .

e Line transient time shall be more than 50μs.

f Start-up delay can be calculated from either the initiation of the converter transition or the removal of the grounded inhibit pin.

Table 9 Electrical Characteristics of BST/100-5-5/D1

No	Items	Symbol	Conditions（Unless otherwise specified, −55℃≤TC≤125℃, VI＝100V±0.5V, CL=0）	Group A Subgroup	Limits Min	Limits Max	Unit
1	Output voltage	VO1	IO1=IO2=0.5A	1	4.95	5.05	V
				2,3	4.85	5.15	
		VO2		1	-5.05	-4.95	
				2,3	-5.15	-4.85	
2	Output Current	IO1	VI=80V～120V	1,2,3	-	500	mA
		IO2			-	500	
	Output ripple voltage	VR1	BW=20MHz，IO1=IO2=0.5A，	1	—	80	
				2,3	—	120	
				1	-	80	

3	（p-p）	VR2	VI=80V、100V、120V	2,3	-	120	mV
4	Voltage regulation rate	SV1	VI=80V→120V，IO1=IO2=0.5A	1,2,3	-	1	%
		SV2			-	1	
5	Load regulation rate	SI1	IO1=IO2=0→0.5A	1,2,3	—	1	%
		SI2			—	1	
6	Input Current	IIN	IOUT=100%, INH is connected with GNDin.	1,2,3	—	5	mA
			IOUT=0%, INH opens.		—	50	
7	Input ripple current （p-p）	IRIP	BW=20MHz, IO1=IO2=0.5A, connected to EMI filter	1,2,3	—	80	mA
8	Input ripple voltage （p-p）	VRIP	BW=20MHz， IO1=IO2=0.5A，connected to EMI filter	1,2,3	—	100	mV
9	Switch frequencyb	fs	IO1=IO2=0.5A	4,5,6	260	360	kHz
10	Efficiency	η	IO1=IO2=0.5A	1	68	—	%
				2,3	65	—	
11	Power dissipation short circuit	PD	Both output short circuit	1	—	4	W
12	Capacitive loadab	CL1	No effect on dc performance	4	—	100	μF
		CL2			—	100	
13	Isolation	RISO	Input to output or any pin to case (except pin 6) at 500V	1	100	—	MΩ

14	Output response to step transient load changes[bc]（peak value）	VLOR1	50% to/from 100% rated load,	4	-400	400	mV
		VLOR2	10% to/from 50% rated load Each output with balanced load.		-400	400	
15	Recovery time step transient load changesbcd	tLOR	50% to/from 100% rated load, 10% to/from 50% rated load Each output with balanced load.	4	—	5	ms
16	Output response to transient step line changes(peak value)[be]	VVOR1	Input voltage VI:80→100V, IO1=IO2=0.5A Input voltage VI：100→80V, IO1=IO2=0.5A	4	-500	500	mV
		VVOR2	Input voltage VI：100→120V, IO1=IO2=0.5A Input voltage VI：120→100V, IO1=IO2=0. 0.5A		-500	500	
17	Recovery time transient step line changes bde	tVOR	Input voltage VI:80→100V, IO1=IO2=0.5A Input voltage VI：100→80V, IO1=IO2=0.5A Input voltage VI：100→120V, IO1=IO2=0.5A Input voltage VI：120→100V, IO1=IO2=0. 0.5A	4	—	5	ms
18	Start-up overshootb	VTO1	Input voltage VI:=0V→100V, IO1=IO2=0.5A	4,5,6	—	300	mV
		VTO2			—	300	

	（peak）						
19	Start-up delayf	tTR	Input voltage VI：0→100V, IO1=IO2=0.5A	4,5,6	—	100	ms
20	Load fault recoverybd	tLF	IO1、IO2 from short circuit to 0.5A	4	—	10	ms
21	Inhibit open voltage	VINH		1	—	15	V
22	Protection power	PW		1	6.5	—	W
23	Cross regulation	SC	One output with 50% load，the other output with 50% ~100% rated load	1,2,3	—	6	%

[a] Capacitive load may be any value from 0 to the maximum limit, without compromising dc parameter.

[b] The parameter is guaranteed by design, and tested only when there is inspection and change in design or process.

[c] Load transition time shall be from 10μs to 15μs.

[d] Recovery time is from the initiation of the transition to the time Vout has returned to steady value within ±1% .

[e] Line transient time shall be more than 50 μ s.

[f] Start-up delay can be calculated from either the initiation of the converter transition or the removal of the grounded inhibit pin.

User Manual

Electrical connection

Test connection is shown in Fig 4.

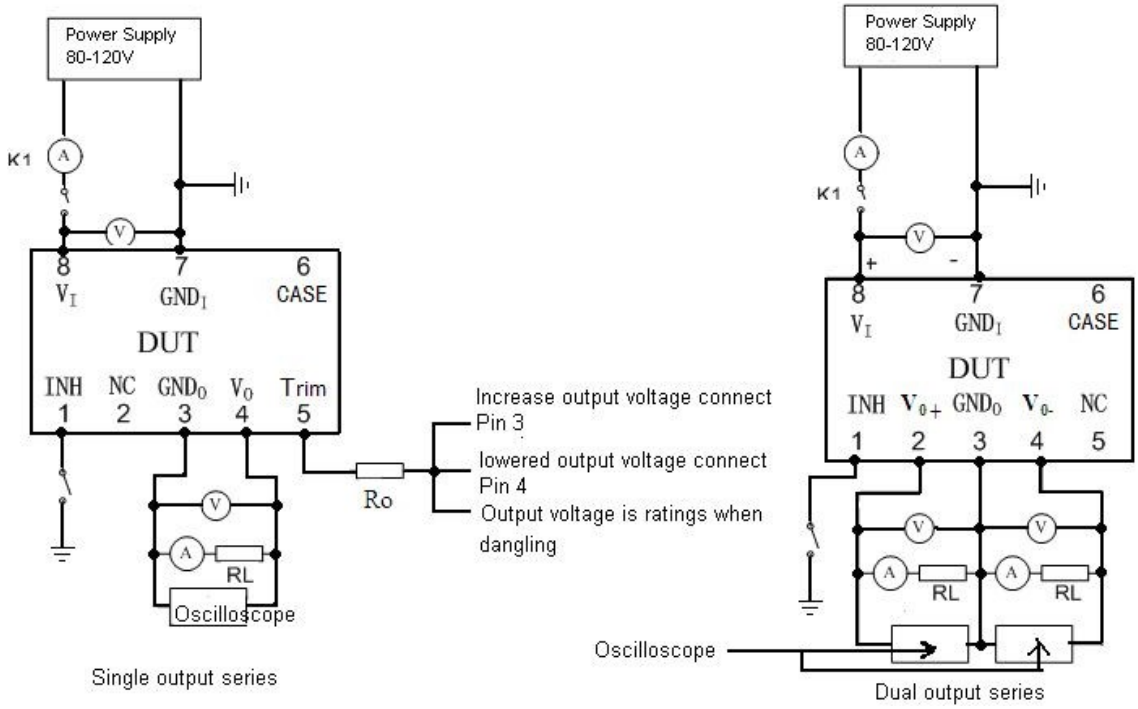


Fig. 4 electrical connection diagram

Inhibit function

The device has inhibit function, inhibiting at low voltage (<0.2V). The device operates normally at high voltage (13V~25V) or when dangling. When the device is inhibited, input current is less than 2mA; output voltage is less than 0.5V.

The device does not output, when the inhibit pin (INH) is grounded directly, or connected with external NPN transistor (set base high level), as shown in Fig. 9. When the inhibit pin is dangled, the voltage is 8.5V-13V DC. The parameter of resistance and capacitance in the Fig. 5 can be appropriately adjusted. The inhibit pin can be dangled when it is not needed.

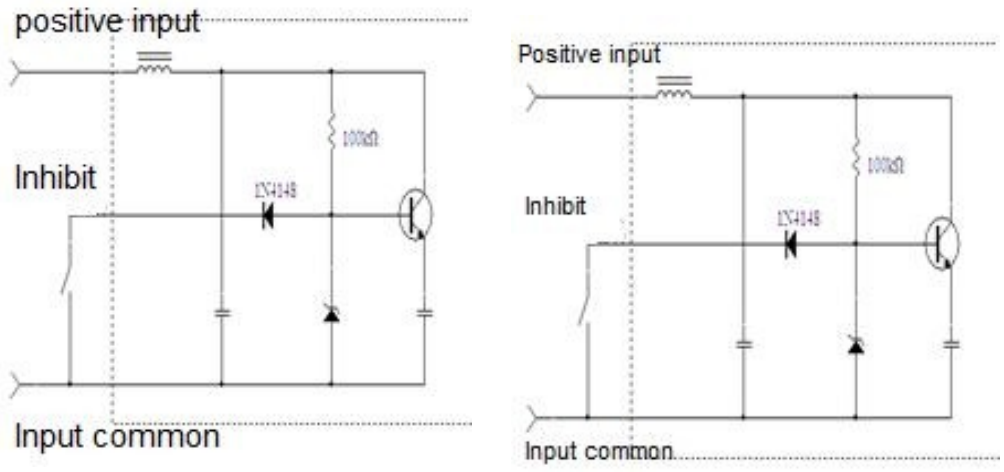


Fig 5 Inhibit pin connection diagram

Short circuit protection function

The series device has short circuit protection function. When output pin shorts, the device is turned into protection state (belching like protection, squeaking sound). Here, output voltage is close to 0V, bus-line current is about 8mA to 20mA, internal power dissipation inside is about 0.8W to 2W when shorts. The parameters above are tested at the bottom of output pin at the normal temperature.

Under-voltage protection function

The series device has under-voltage protection function. When input voltage is under 60V±5V, the device does not have output voltage.

Surge protection capability

Surge protection voltage of the series device is 160V/1ms. It is recommended for user to consider input port high voltage.

Design of surge protection circuit at front end

LC filter circuit is used at input port inside of the device. At the moment of power start-up, there is inevitably high surge current because ESR of capacitor is small (mΩ level). So it is recommended for user to add surge protection circuit or select EMI filter with surge protection circuit.

Surge protection circuit is shown in Fig. 6:

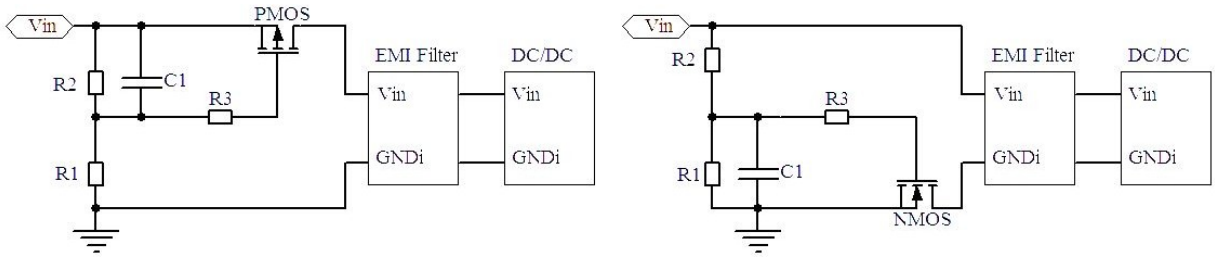


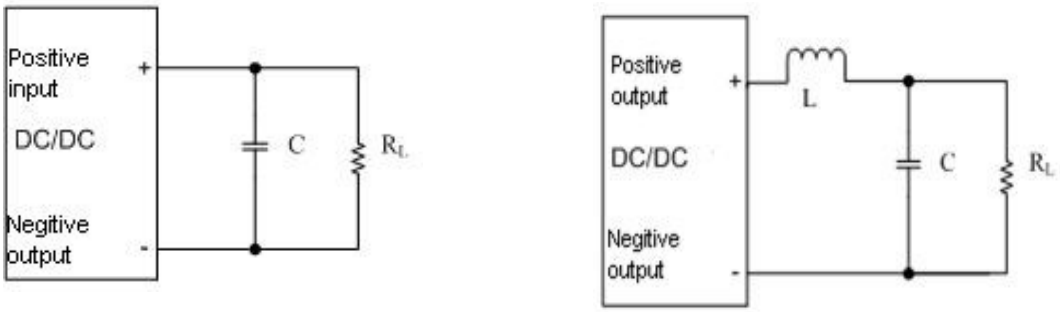
Fig. 6 Surge protection circuit

It is recommend to use R1 =95k Ω, R2=10k Ω, R3=20 Ω, C1 =1 μF. Charge and discharge time can be controlled by changing the value of C1 . The withstand voltage of P channel and N channel MOSFET shall more than 200V. Current should be considered according to the bus bar current, coupled with grade 1 derating design. It is recommended that input voltage rise time of DC/DC converter shall be more than 1ms. The specific value of the capacitance C1 shall be set by the user according to the actual system application.

Design of output filter at back-end

LC filter circuit is used internally. If output ripple can not meet the requirements of the system, filter circuit can be redesigned at the output port of DC/DC converter in order to reduce the ripple. Several recommended filter circuits are as follows.

Fig 7 Connected with capacitor Fig 8 Connected with LC fi l ter



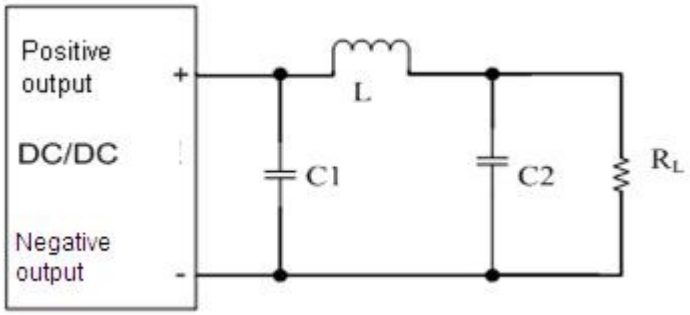
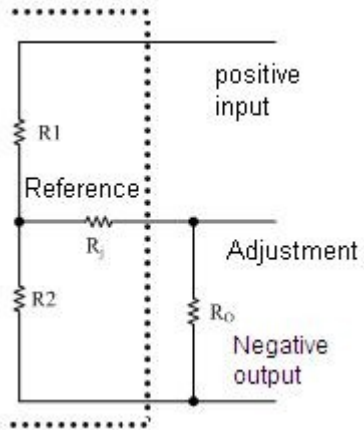
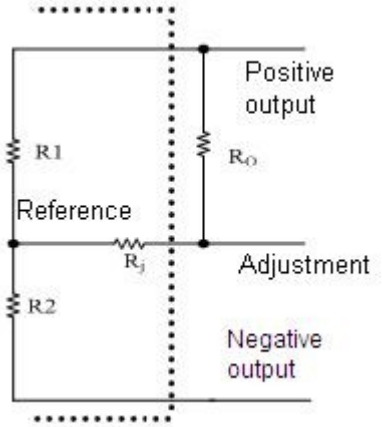


Fig.9 Connected with Π type filter

Capacitor shall be closely mounted to the load side as possible, capacitance of the external capacitor shall be less than capability of the converter with capacitive load; The inductance of L inductor can be adjusted accordingly.

Use of single output adjustment end





（a） Output voltage up （b） Output voltage down Fig 10 Adjustment end of single output connection

As shown in Fig. 10, R1 , R2, Rj are internal resistors, Ro is an external resistor, fine- trimming the output voltage of DC/DC converter. First potentiometer is used to debug output voltage, and then replaced with precision resistor. The resistance is no less than 1/10 W.

Table 2 Selection of resistance adjustment end of BST/100-5-5/SP

BST/100-15-5/SP Output voltage up VOH						BST/100-5-5/SP Output voltage down VOL					
R1	R2	Vref	Rj	RO	VOH	R1	R2	Vref	Rj	RO	VOL
（K）	（K）	（V）	（K）	（K）	（V）	（K）	（K）	（V）	（K）	(K)	(V)
3.5	1.5	1.5	8.5	90	5.05	3.5	1.5	1.5	8.5	250	4.95
				45	5.1					105	4.9
				26	5.15					70	4.85
				18	5.2					50	4.8
				12.5	5.25					37	4.75
				9	5.3					29	4.7
				6.5	5.35					23	4.65
				4.5	5.4					19	4.6
				3.2	5.45					15	4.55
				2.1	5.5					12.5	4.5

Table 3 Selection of resistors at adjustment end of BST/100-15-5/SP

BST/100-15-5/SP Output voltage up VOH						BST/100-15-5/SP Output voltage down VOL					
R1	R2	Vref	Rj	RO	VOH	R1	R2	Vref	Rj	RO	VOL
（K）	（K）	（V）	（K）	（K）	（V）	（K）	（K）	（V）	（K）	(K)	(V)
				80	15.15					800	14.9
				36	15.3					390	14.7
				21	15.45					255	14.6
				13.5	15.6					185	14.4
				9	15.75					145	14.3
				6	15.9					117	14.1
				3.9	16.05					98	14
				1.4	16.3					83	13.8
9				0.3	16.45					72	13.7
	1	1.5	9	0.03	16.5	9	1	1.5	9	63	13.5

Table 4 Selection of resistors at adjustment end of BST/100-3R3-5/SP

BST/100-15-5/SP Output voltage up VOH						BST/100-5-5/SP Output voltage down VOL					
R1	R2	Vref	Rj	RO	VOH	R1	R2	Vref	Rj	RO	VOL
（K）	（K）	（V）	（K）	（K）	（V）	（K）	（K）	（V）	（K）	(K)	(V)
				500	3.33					600	3.27
				250	3.36					300	3.24
				150	3.39					180	3.21
				100	3.42					120	3.18
				65	3.45					80	3.15
				45	3.48					55	3.12
				30	3.51					35	3.09
				20	3.54					25	3.06
				11	3.57					15	3.03
12	10	1.5	55	6	3.6	12	10	1.5	55	6	3

Typical output waveform

Start-up delay/start-up overshoot（TC=25℃，Vin=100V±0.5V，full load）

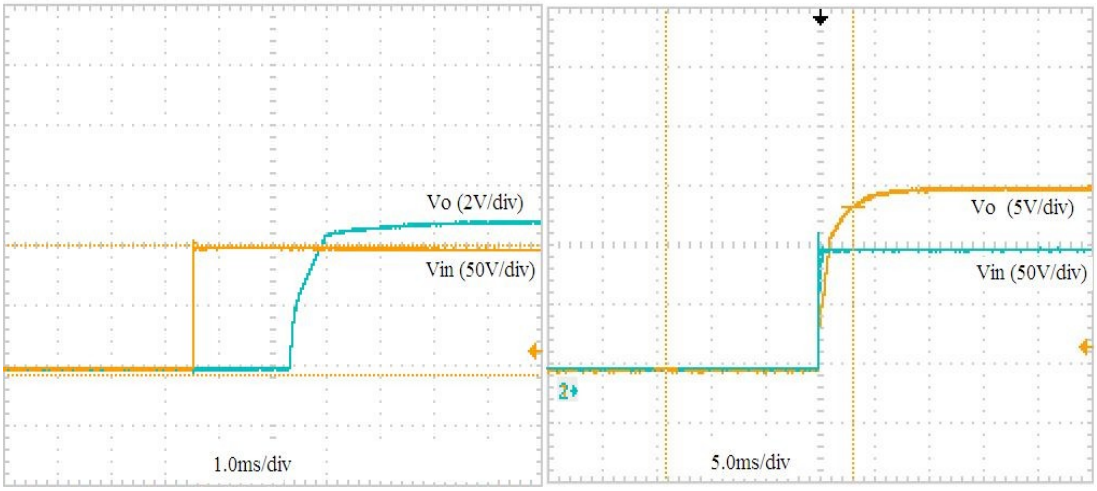


Figure11 BST/100-5-5/SP Figure12 BST/100-15-5/SP

Start-up delay/start-up overshoot Start-up delay/start-up overshoo

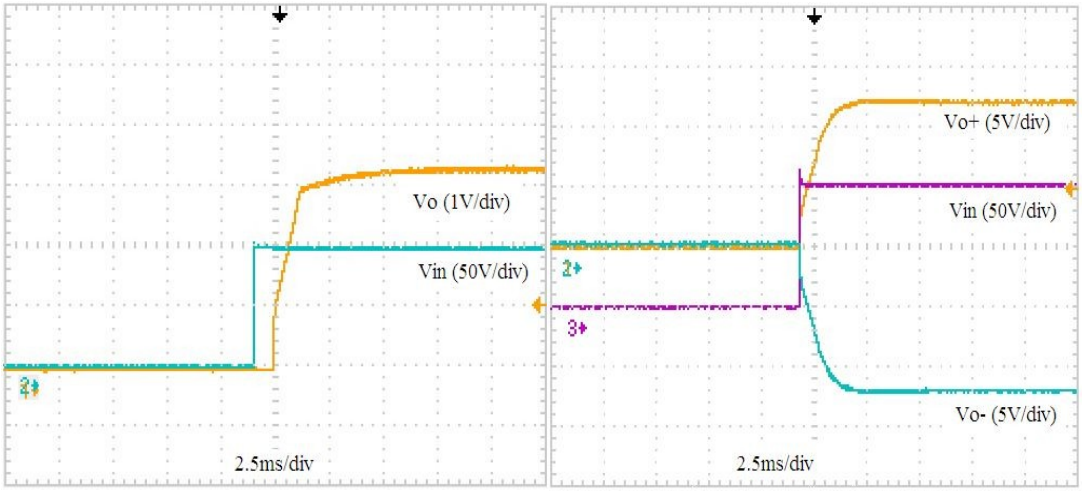


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Fig.13 BST/100-3R3-5/SP Fig. 14 BST/1010-12-5/D1

Start-up delay/start-up overshoot Start-up delay/start-up overshoot

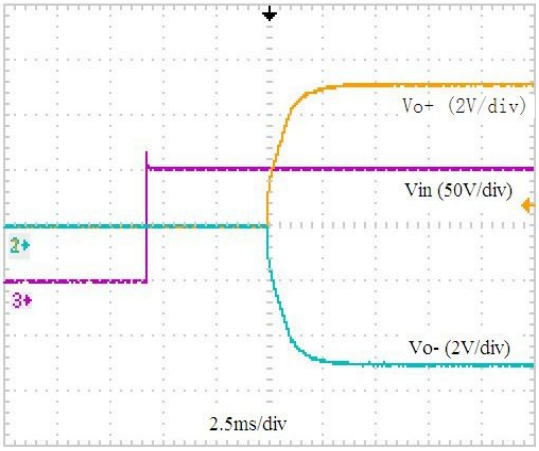


Fig. 15 BST/100-12-5/D1 Start-up delay/start-up overshoot

Load step curve（TC=25℃ Vin=100V±0.5V)

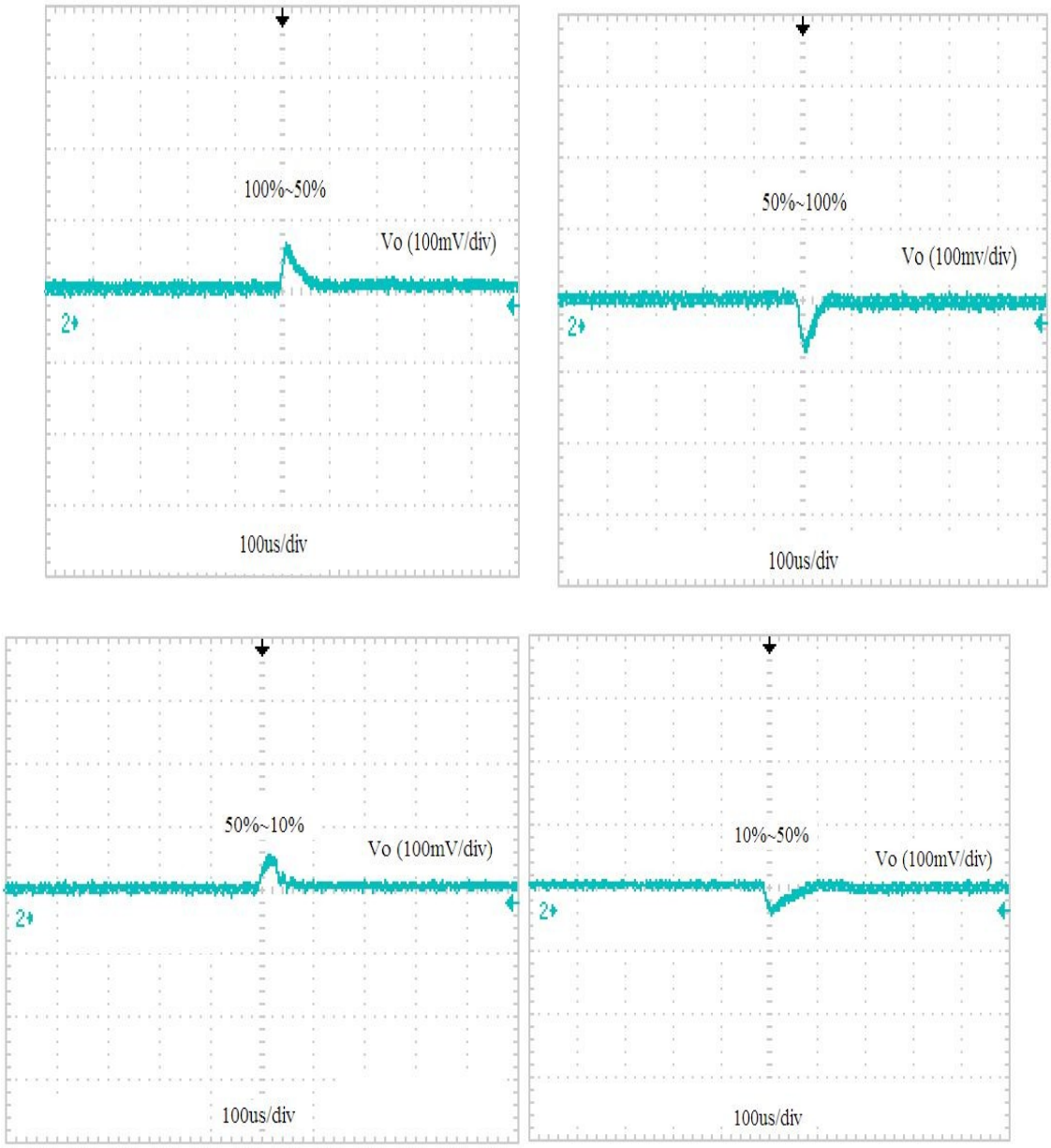


Fig. 16 Load step curve BST/ 100 - 5 - 5 / SP

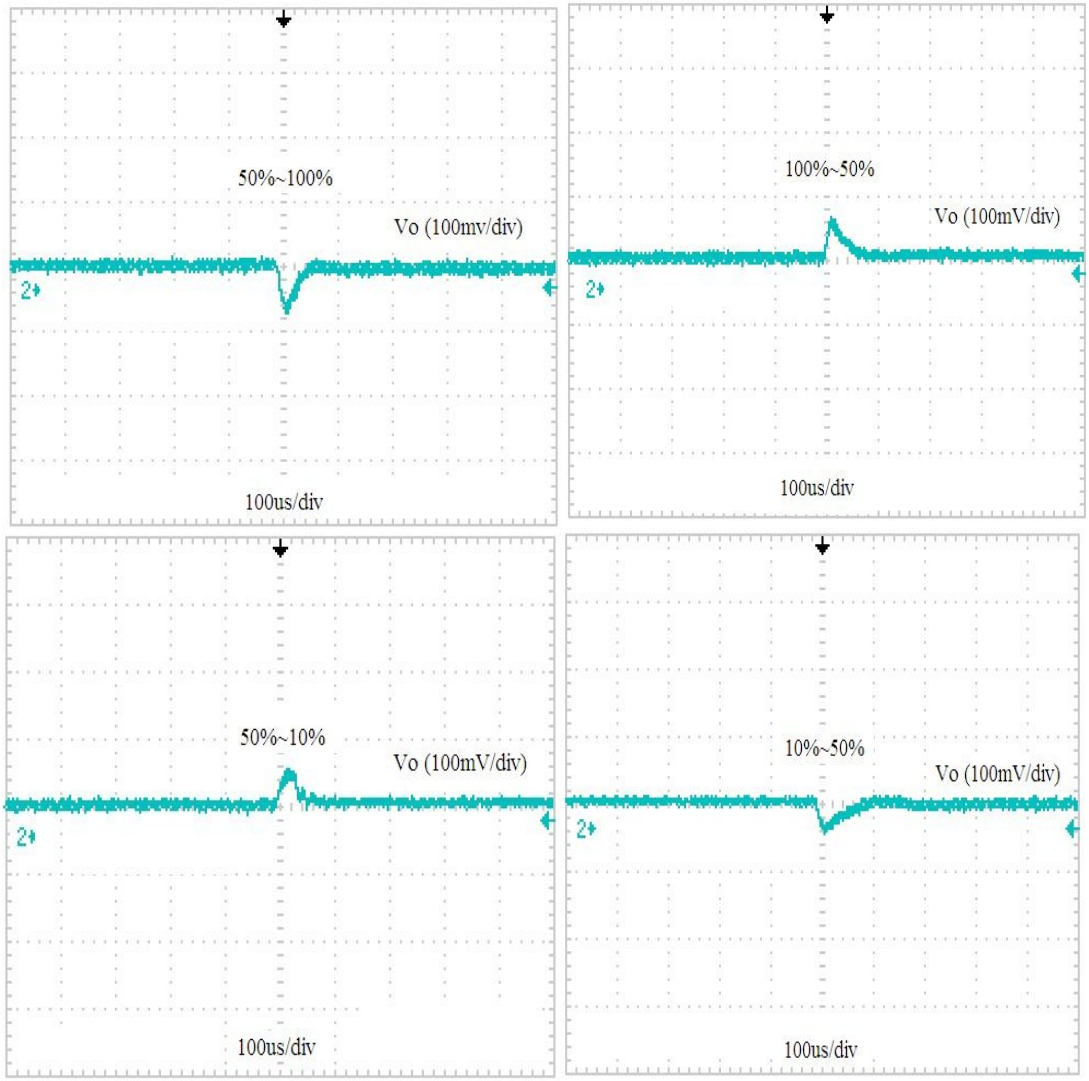


Fig. 17 Load step curve of BST/ 100 - 15 - 5 / SP

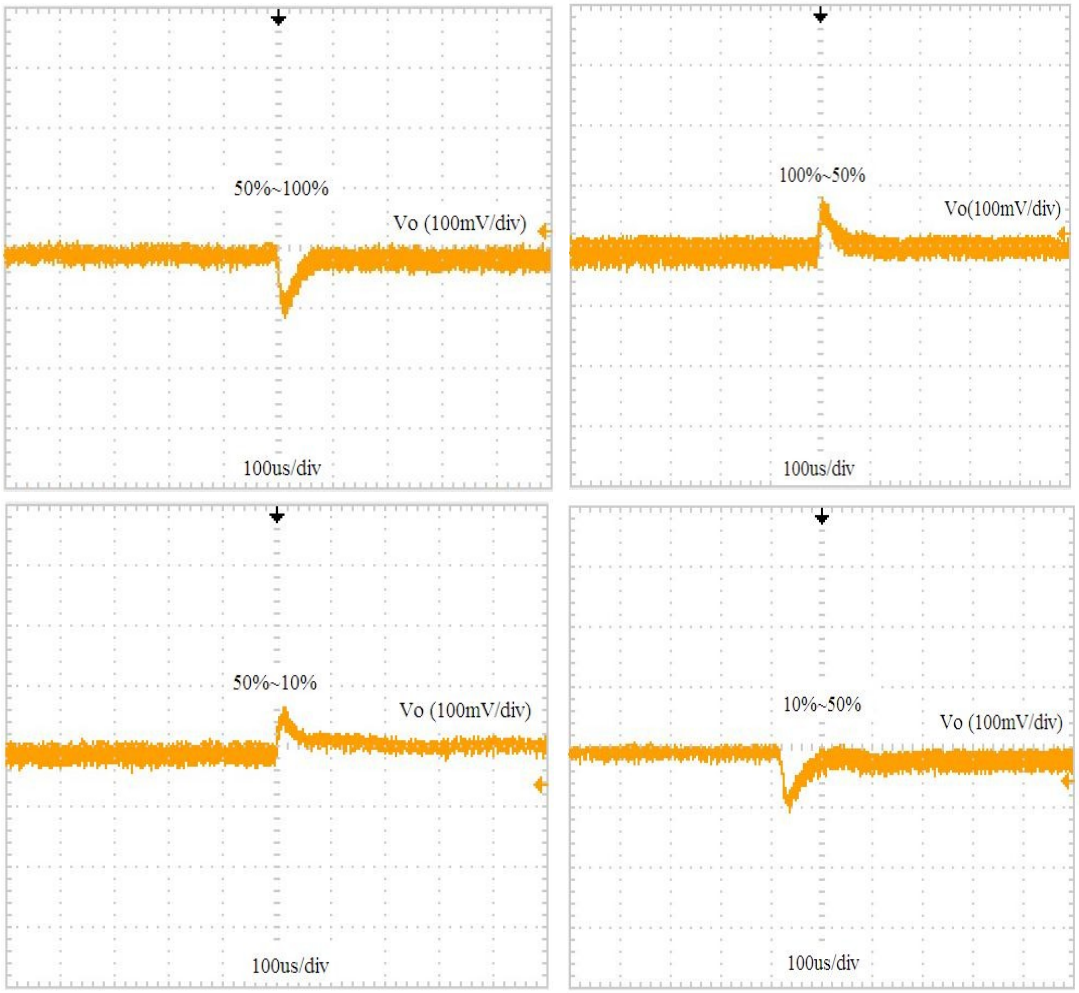


Fig. 18 Load step curve of BST/ 100 - 3 R 3 - 5 / SP

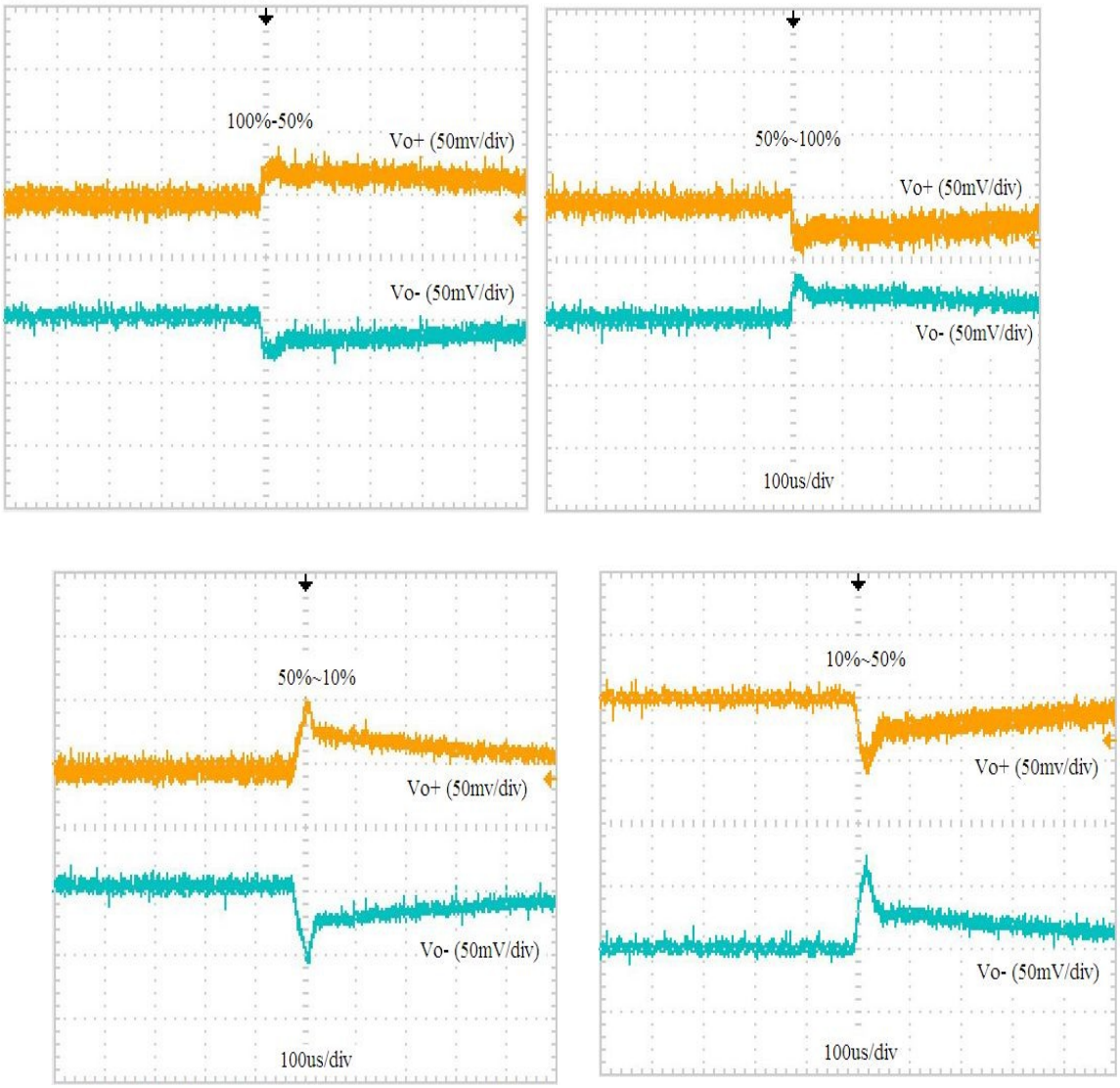
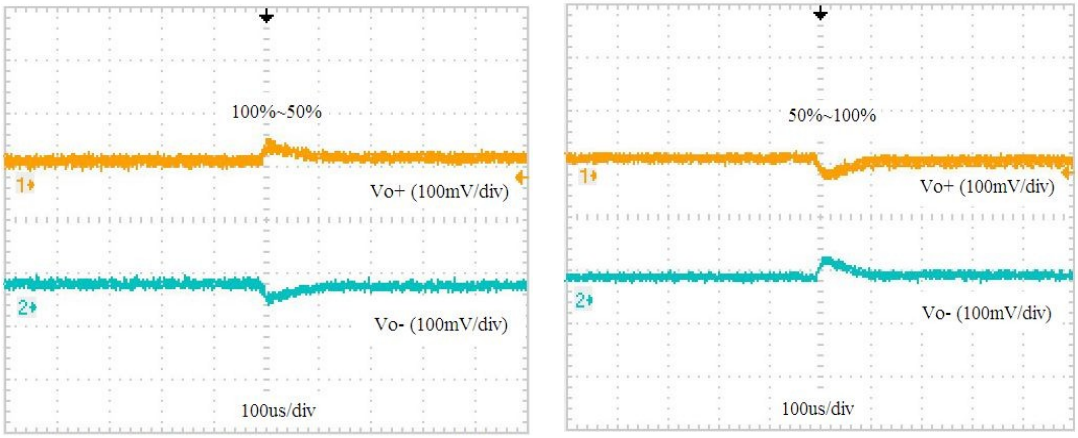


Fig. 19 Load step curve of BST/ 100 - 12 - 5 / D 1



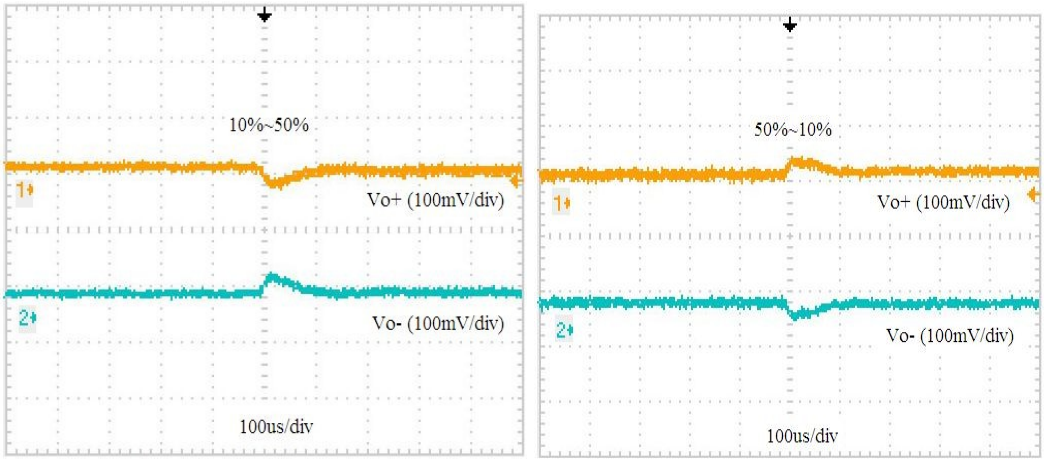


Fig. 20 Load step curve of BST/ 100 - 5 -5 / D 1

Line step curve（TC=25℃，full load）

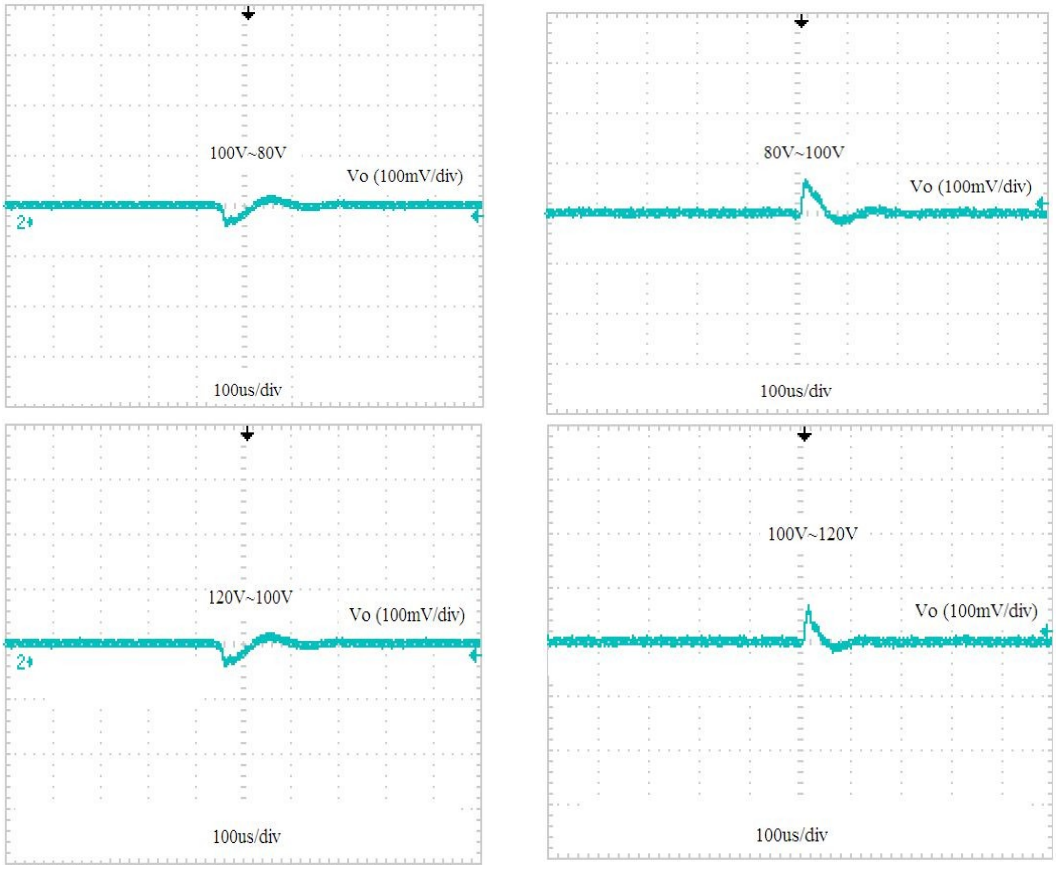


Fig. 21 Line step of BST/ 100 - 5 - 5 / SP

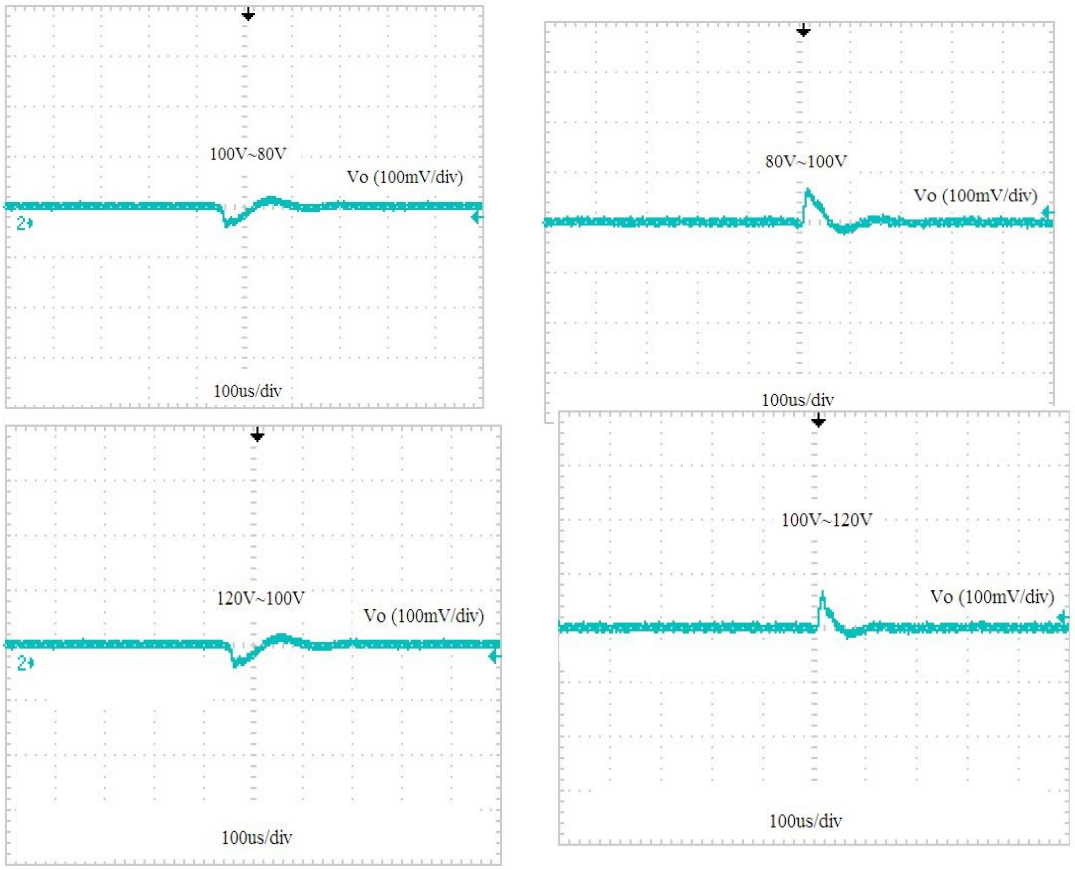


Fig. 22 Line step of BST/ 100 - 15 - 5 / SP

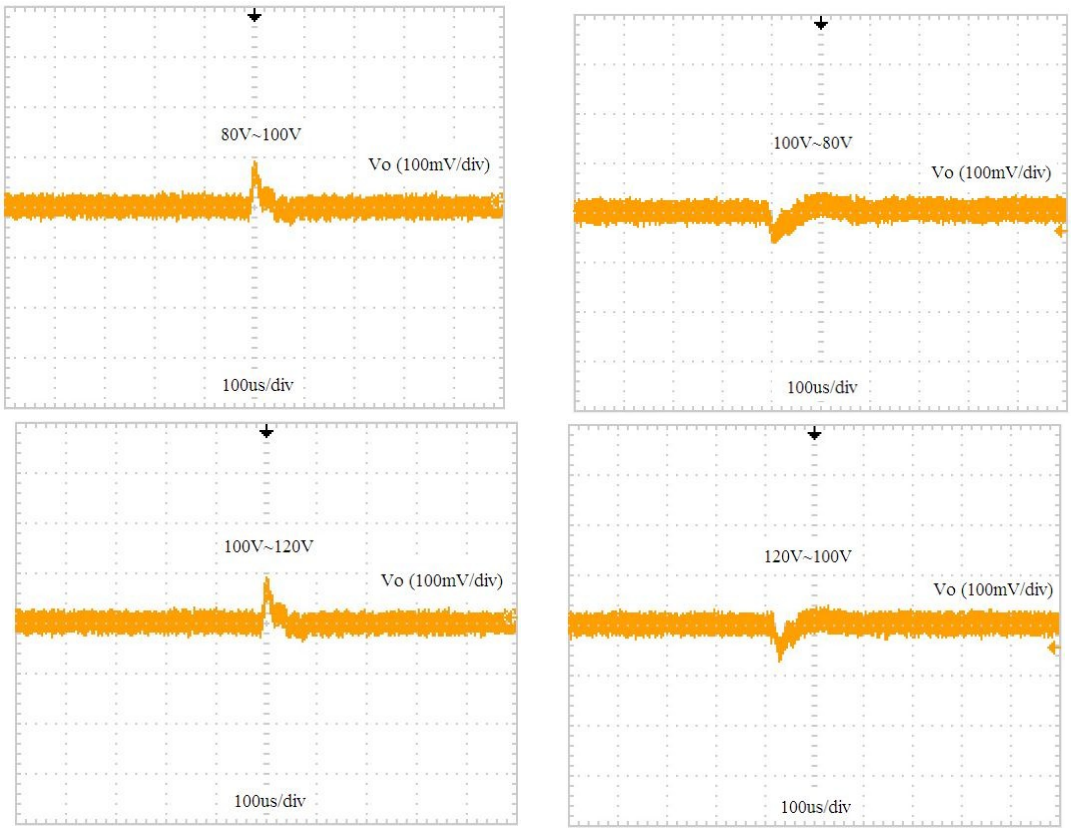


Fig. 23 Line step of BST/ 100 - 3 R 3 - 5 / SP

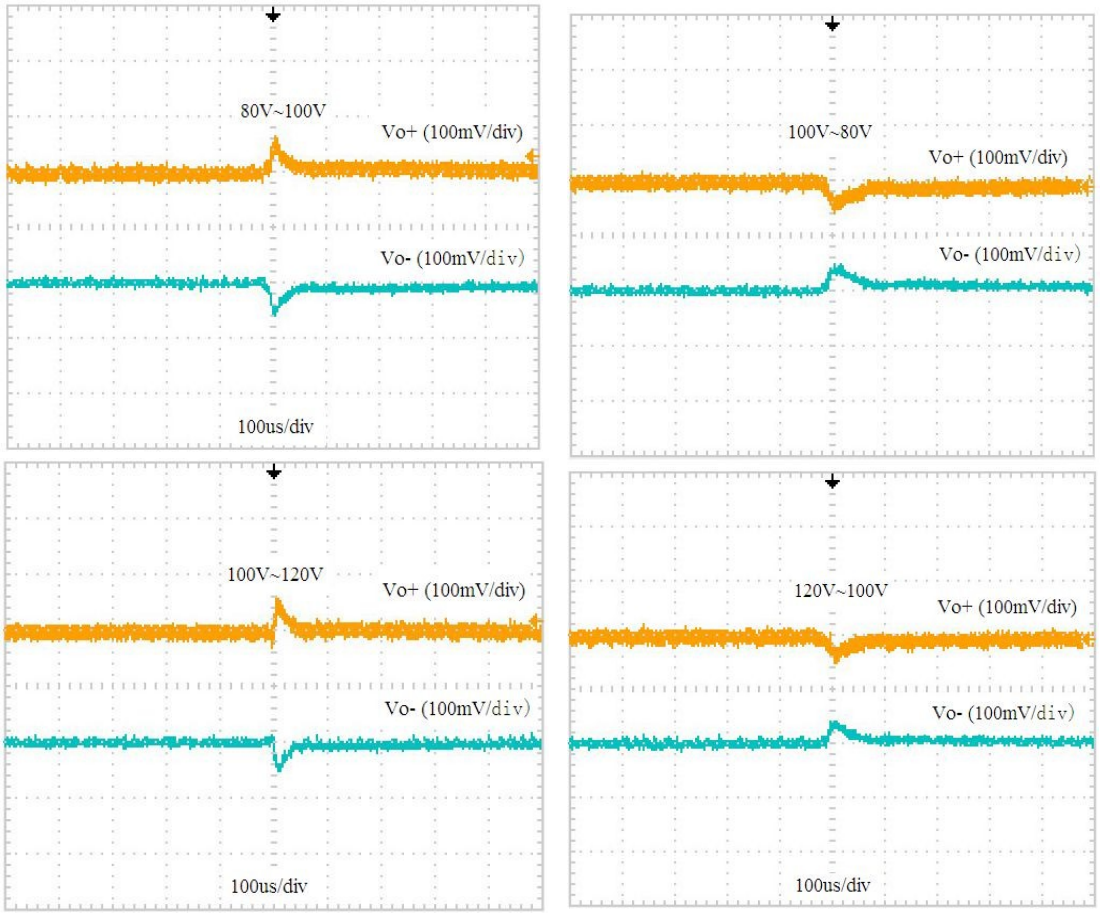
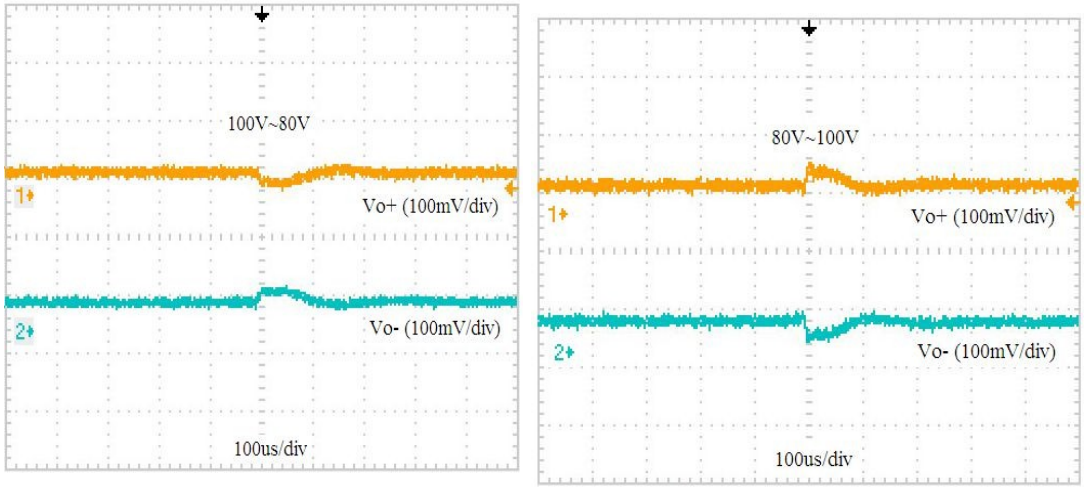


Fig. 24 Line step of BST/ 100 - 12 - 5 / D1



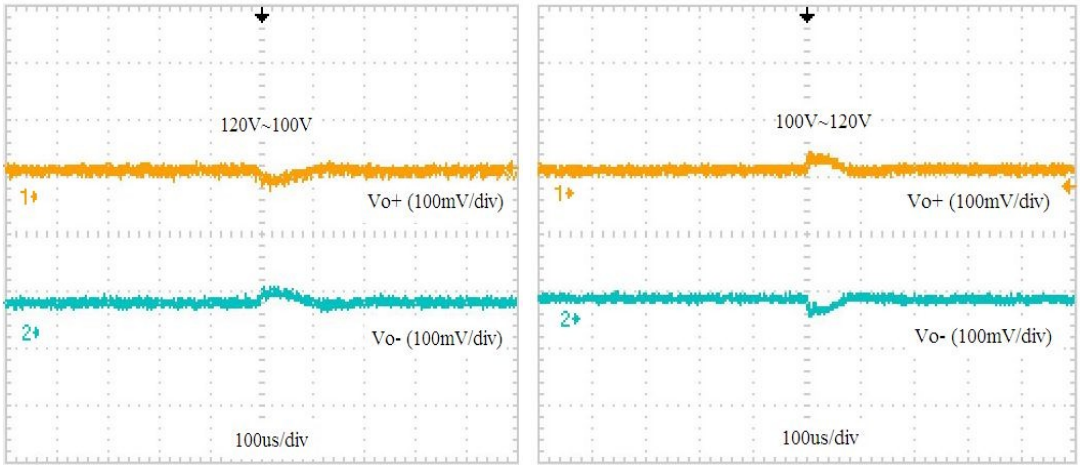


Fig. 25 Line step of BST/ 100 - 5 -5 / D1

Output efficiency curve

Output power- efficiency curve （TC=25℃，Vin=100V±0.5V）

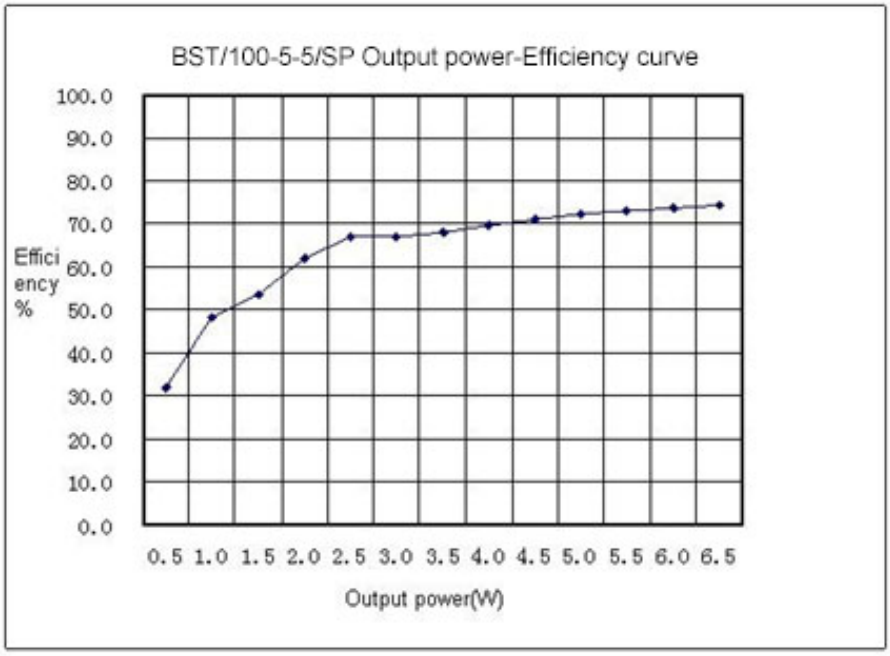


Fig. 26 Output power- efficiency curve of BST/ 100 - 5 - 5 / SP

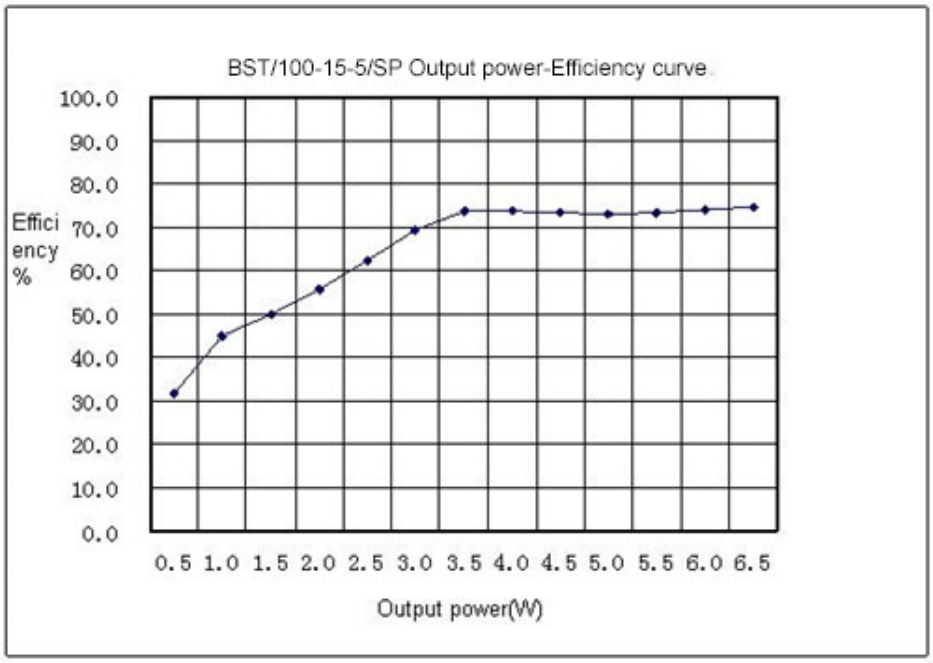


Fig. 27 Output power- efficiency curve of BST/ 100 - 15- 5 / SP

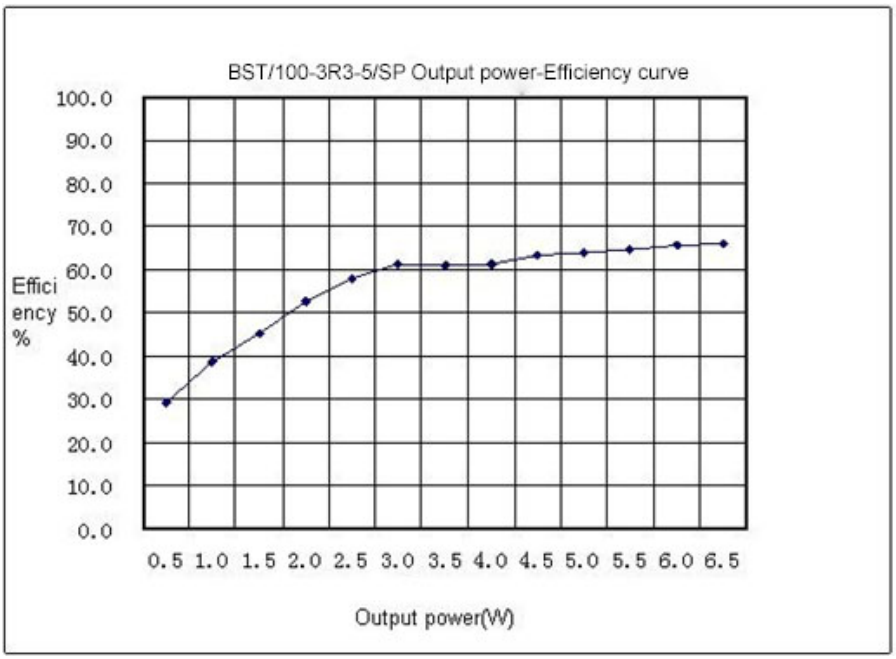


Fig. 28 Output power- efficiency curve of BST/ 100 - 3R 3 -5 / SP

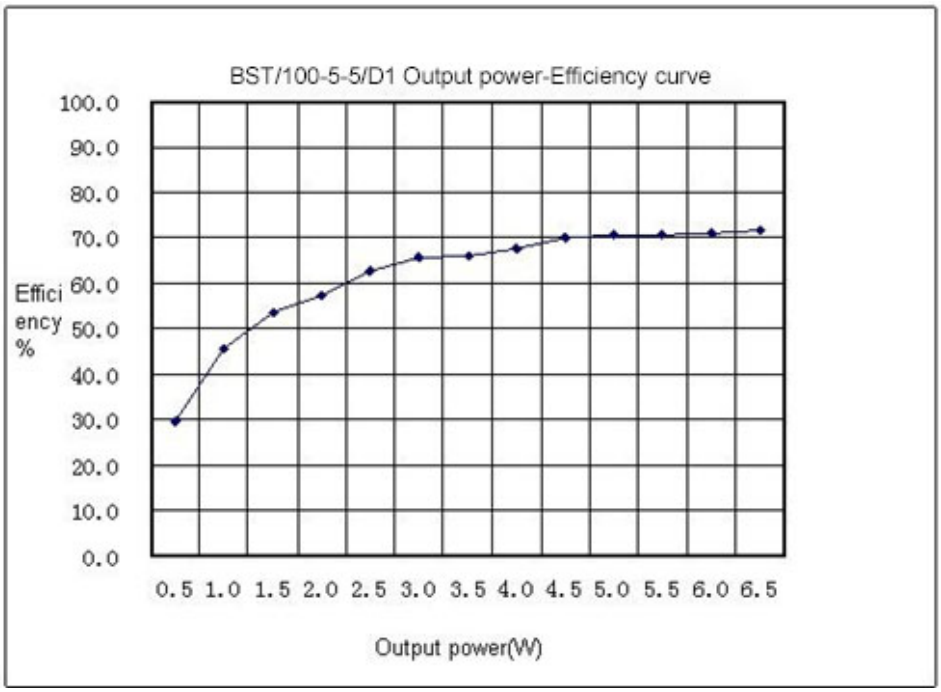


Fig 29 Output power- efficiency curve of BST/ 100 - 5 - 5 / D1

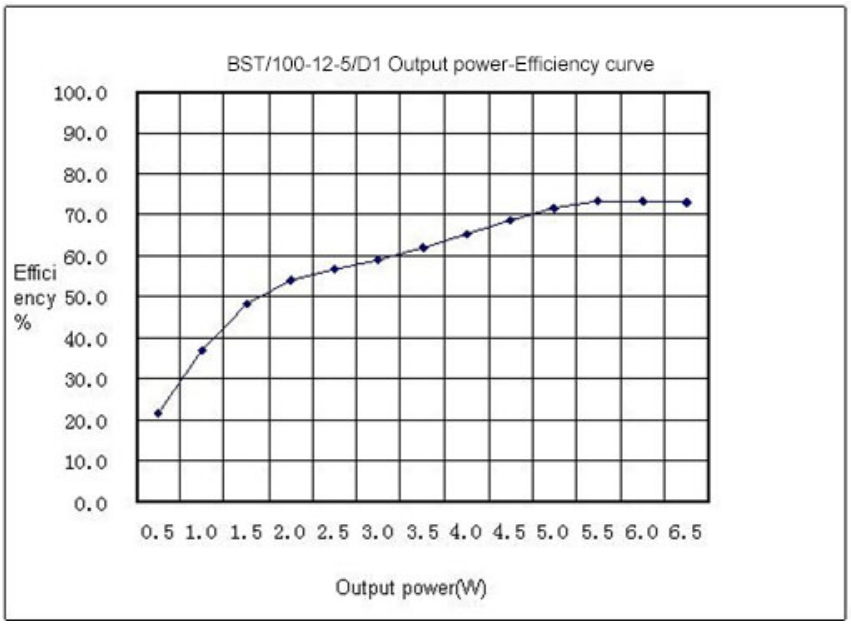


Fig. 30 Output power- efficiency curve of BST/ 100 - 12 -5 / D1

Input voltage- efficiency curve （ TC=25 ℃， full load ）

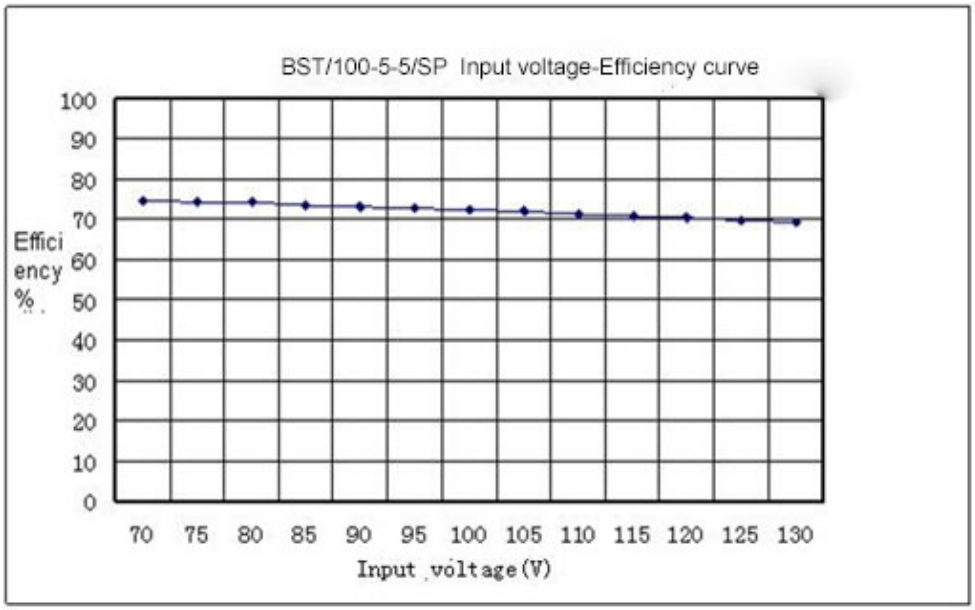


Fig. 31 Input voltage- efficiency curve of BST/ 100 - 5 - 5 / SP

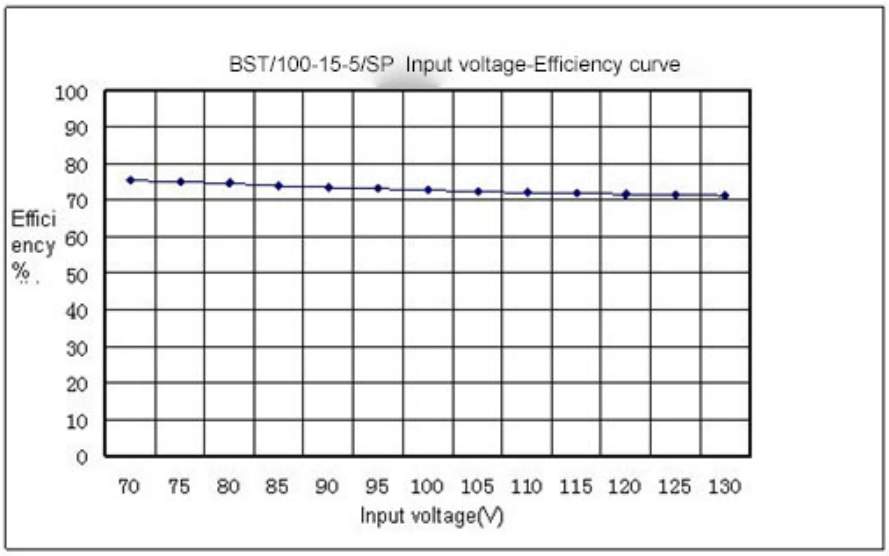


Fig. 32 Input voltage- efficiency curve of BST/ 100 - 15- 5 / SP curve

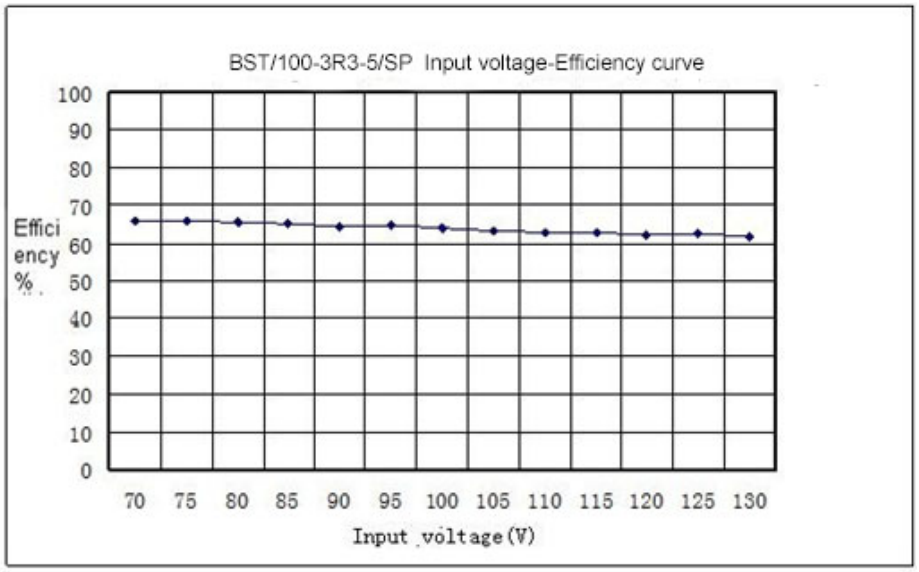


Fig. 33 Input voltage- efficiency curve of BST/ 100 - 3R 3 -5 / SP

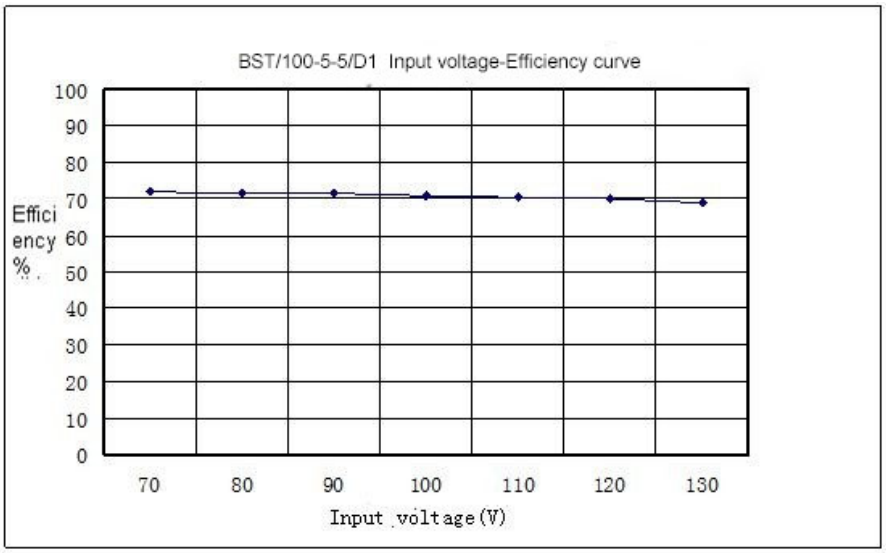


Fig. 34 Input voltage- efficiency curve of BST/ 100 - 5 - 5 / D1

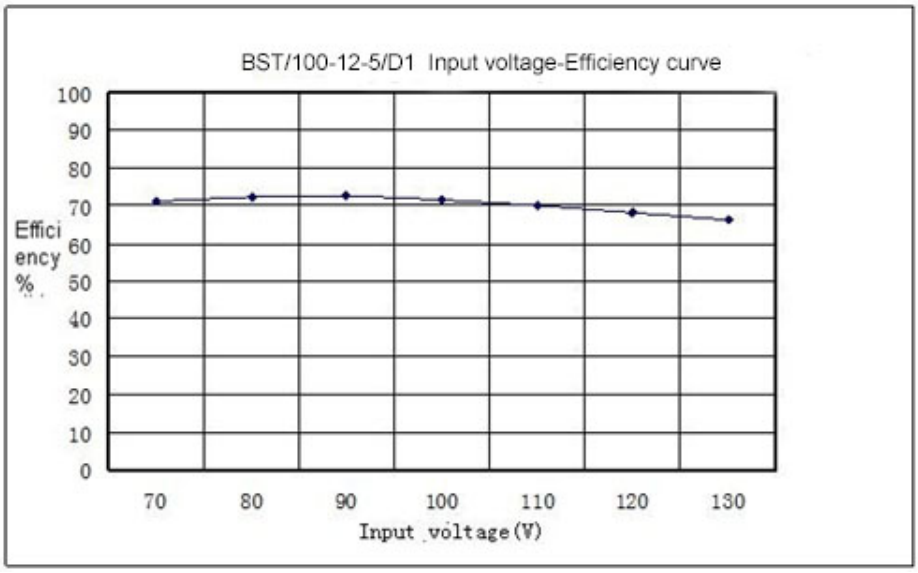
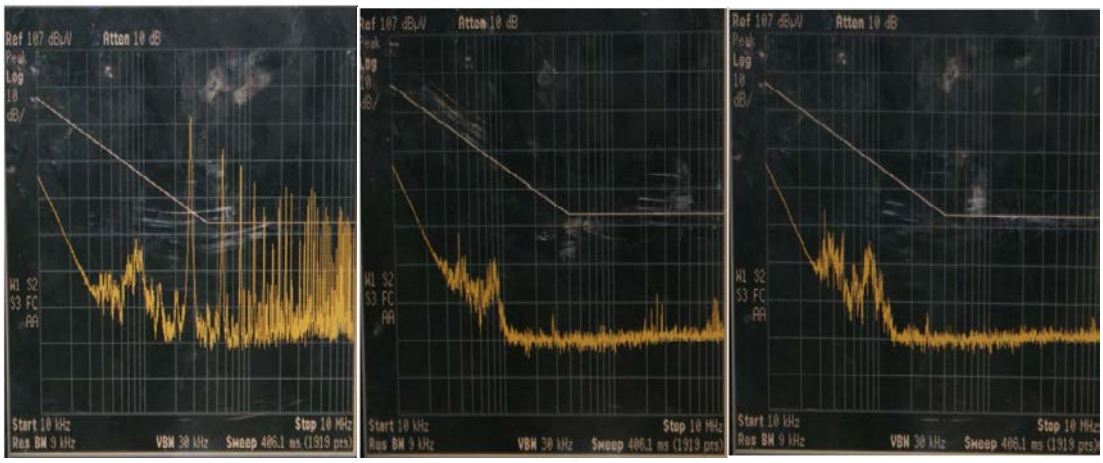


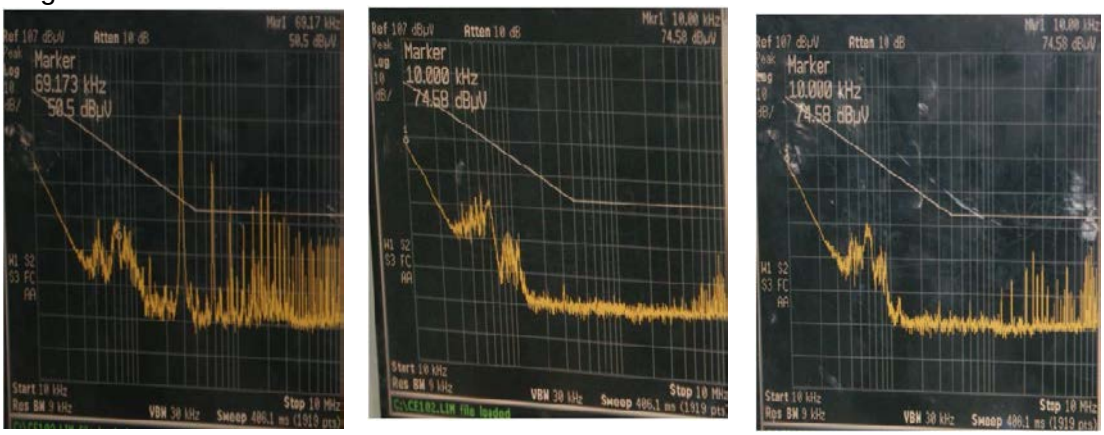
Fig. 35 Input voltage- efficiency curve of BST/ 100 - 12 -5 / D1

Effect of CE102 after using EMI filter

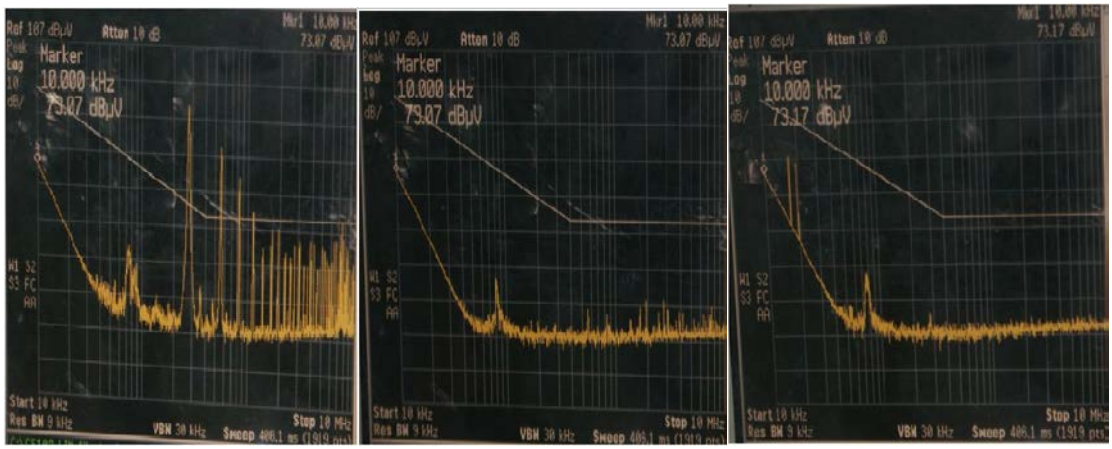


Without filter With BST100-461-80 filter With BST100-461-300 filter

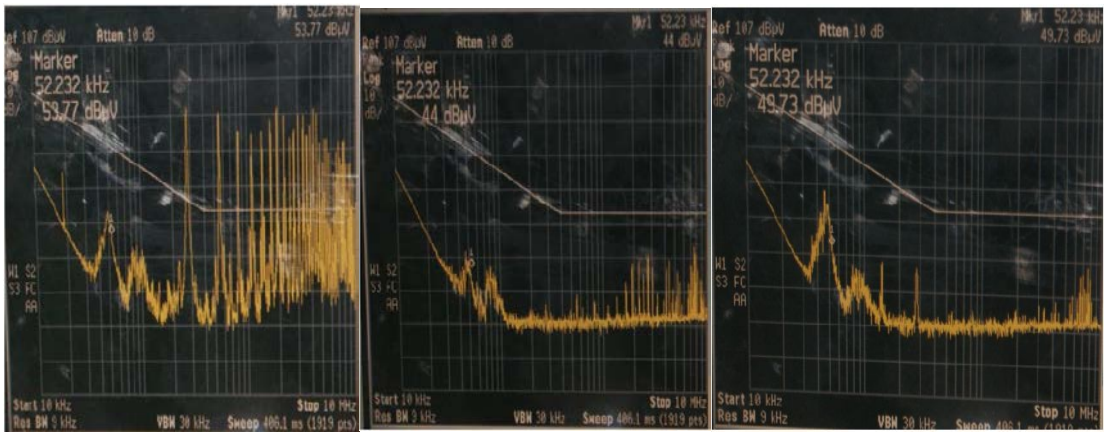
Fig. 36 BST/ 100 - 5 -5 /SP



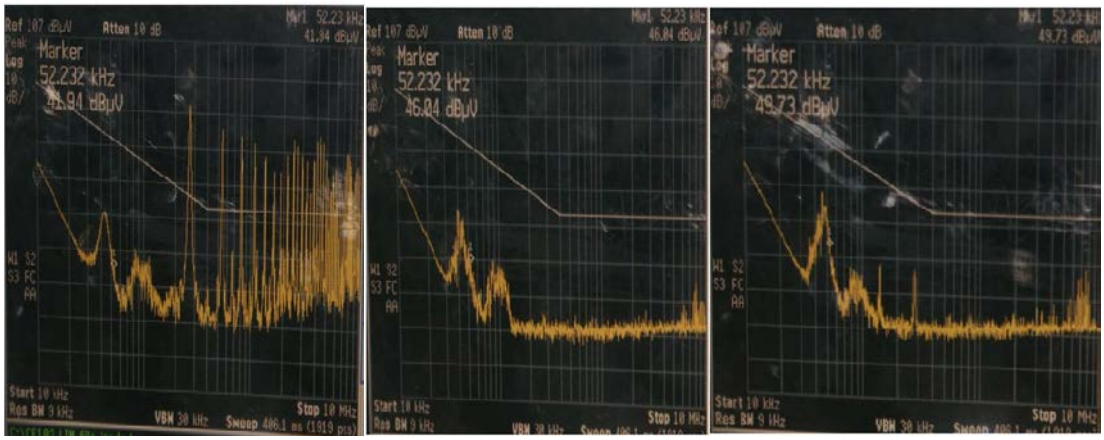
Without filter With BST100-461-80 filter With BST100-461-300 filter Fig. 37 BST/ 100 - 15 -5 /SP



Without filter With BST100-461-80 filter With BST100-461-300 filter Fig. 38 BST/ 100 - 3R 3 -5 /SP



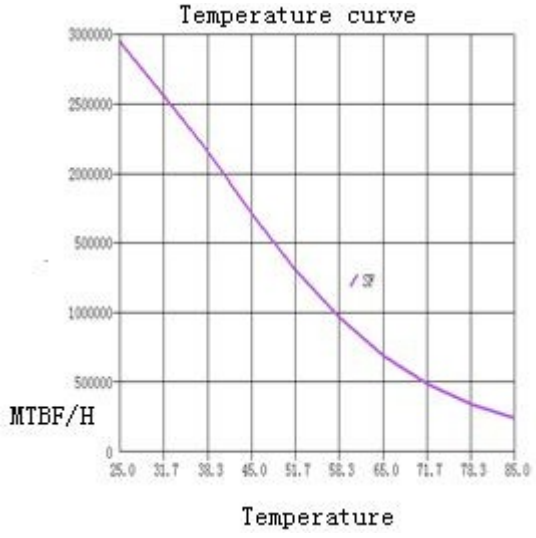
Without filter With BST100-461-80 filter With BST100-461-300 filter Fig. 39 BST/ 100 - 12 -5 /D 1



Without filter With BST100-461-80 filter With BST100-461-300 filter

Fig. 40 BST/ 100 - 5 -5 /D 1

MTBFcurve



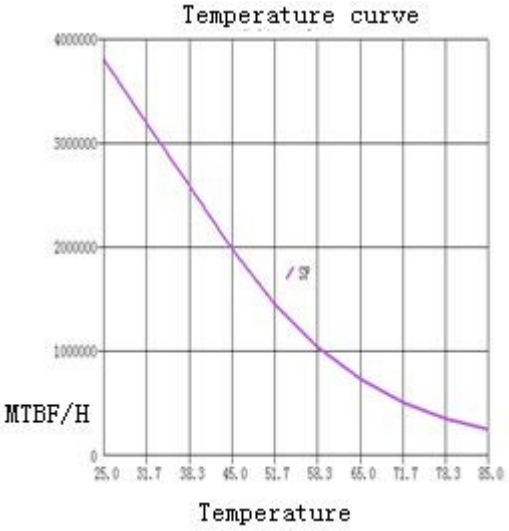
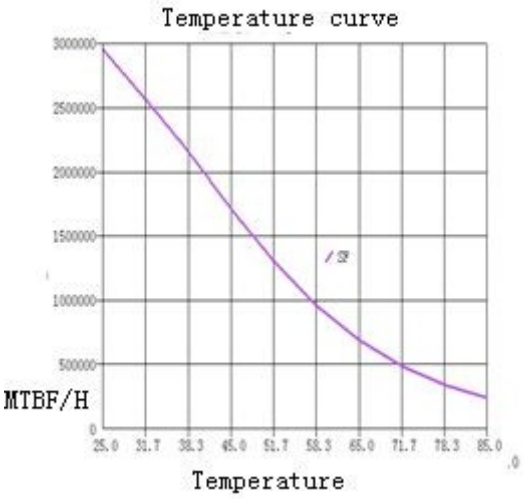


Fig. 41 BST/ 100 - 5 - 5 / SP Fig. 42 BST/ 100 - 15 - 5 / SP



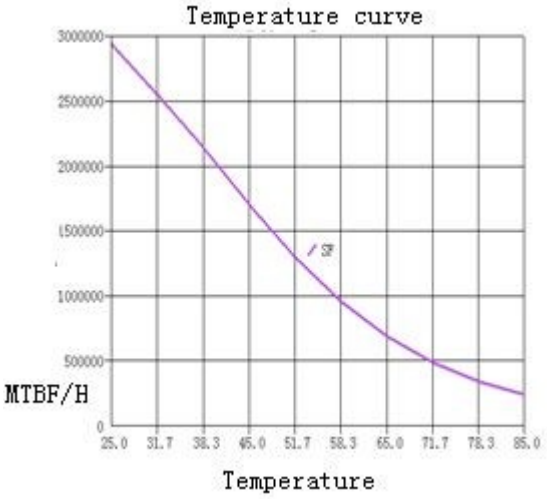


Fig. 43 BST/ 100 - 3 R 3 - 5 / SP Fig. 44 BST/ 100 - 12 - 5 / D 1

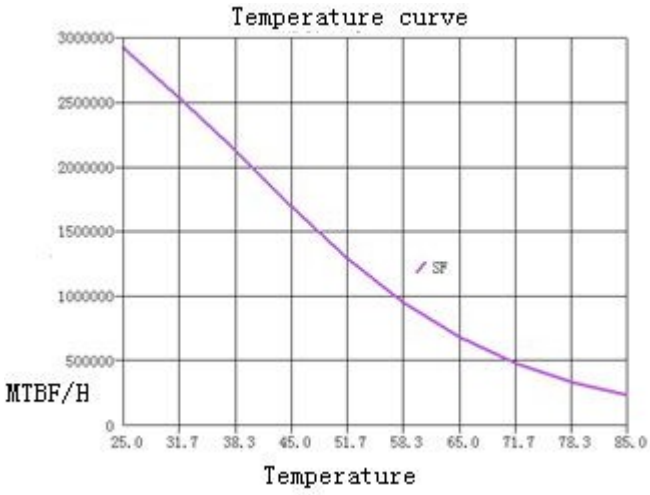


Fig. 45 BST/ 100 - 5 - 5 / D 1

Internal thermal resistance

Metal case of this series devices are cold rolled steel which has higher thermal conductivity. Internal thermal resistance is shown in Table 5.

Table 5 Internal thermal resistance

Model	Internal thermal resistance（℃/W）	Heat sink dimensions (mm3)	Power(w）	Heat sink material
BST/100-5-5/SP	4.7	60×70 ×2	5	Cu
BST/100-15-5/SP	4.8	60×70 ×2	5	Cu
BST/100-3R3-5/SP	4.9	60×70 ×2	5	Cu
BST/100-5-5/D1	4.5	60×70 ×2	5	Cu
BST/100-12-5/D1	4.5	60×70 ×2	5	Cu

Application notes

Case pins shall not be bent to avoid bruising insulators to affect device hermeticity.

Check the polarity of input power line before powering on so as to avoid permanent failure caused by powering on suddenly.

Check load conditions carefully during operation to avoid instability.

Take electrostatic protection measures during storing, transporting, installing and debugging.

Observe “User Manual” during storing, operation and soldering.

Keep away from high voltage input terminal during operation.

Heat sink shall be used with the device to keep the case temperature below 125 ºC. The bus voltage rise time shall be more than 1ms.